RESUME

Venkateshseerapu
Latchayyapeta,
Seethanagaram (Mandal),
Vizianagaram (Dist),
Andhra Pradesh.
PIN: 535573

Email Id: venkateshseerapu2019@gmail.com
Mobile No: 9666594294, 8919421273

Career Objective:

To work with a professional managed organization where I can take challenges in order to widen my career horizons and contribute my best for the progress of organization.

Academic Qualifications:

Class	Discipline/ Specialization	Board/ University	Institution	Year of passing	% of Marks
Ph.D. (Pursuing)	VLSI	Andhra University	Andhra University	-	-
M.Tech	VLSI	JNT University, Kakinada	MVGR college of engineering	2012	75.64
B.Tech	Electronics & Communication Engineering	JNT University, Kakinada	Gokul Institute of Technology and sciences	2009	70.99
Intermediate	M.P.C	Board of Intermediate Education	Sai Vikas Junior College	2005	82.6
X Class	S.S.C	Board of Secondary Education	Abhyudaya Convent & High School	2003	85

Experience:

- Presently Working as Asst. Professor in **Engineering and Technology Program, Gayatri Vidya Parishad College for Degree and PGCourses (A), Visakhapatnam** from 16/06/2014 to till date
- Worked as Asst. Professor in **VITS Group of Institutions, Visakhapatnam** from 28/11/2012 to10/06/2014.

Technical Skills:

- C Language
- Verilog, System Verilog
- Designing Software: Mentor Graphics, Lab VIEW, MATLAB, Tanner Tools, Xilinx, Spice Software's.

Academic Projects:

- **B.Tech Project:**

  Accident Identification Using GPS & GSM

- **M.Tech Project:**

  Implementation of Optimized Reconfigurable Built in Self Repair Scheme for RAM's In SOC

Publications:

1. S. Venkatesh[1], V. Dhakshitha[2], Subham Panda[3], P. Devi[4], R. Kishore[5] "**STABILITY ANALYSIS OF 6T CMOS SRAM CELL USING TANNER EDA**" published at: **The International journal of analytical and experimental modal analysis**, Volume XVI, Issue IV, April/2024, Page No: 927-931 DOI:18.0002.IJAEMA.2024.V16I4.200001.0156859717907292.

2. Venkatesh Seerapu, Krishna Veni Sahukara, "**Power Consumption Analysis of 6T, 7T, 8T and 9T SRAM Cell Topologies using 180nm, 130nm, 90nm and 45nm Technology Nodes**" presented at: **1st National Conference on Design Thinking: Trans-Disciplinary Challenges & Opportunities**, 7-8 July 2023

3. [1]Venkatesh Seerapu, [2]S. V. Vishal, [3]N. Sridar, [4]K. Sagar, [5]M. Charan, "***Fingerprint Identification Based Attendance System with SMS Notification***" published at: **International Journal Of Creative Research Thoughts - IJCRT**, Volume 10 Issue 7, July 2022.

4. K. Damodar Sai Kiran, I. Satish, G. Sai Kiran, J. Sagar , S. Venkatesh, "***Robotic Arm Using Esp32 Microcontroller With Browser Control***" published at: **International Journal for Research in Applied Science & Engineering Technology (IJRASET)**, Volume 5 Issue 7, July 2021.

5. S. Venkatesh[1] , K. Pavankumar[2] , K. Saikiran Reddy[3] , P. Praveen Kumar[4] , G. Venkatesh[5], "***Leakage Reduction in 180nm CMOS Full Adder using Modified Lector Technique***" published at: **International Journal of Scientific Research in Engineering and Management (IJSREM)**, Volume 7 Issue IV, Apr 2019.

6. Venkatesh Seerapu1, N Sowmya2 and Priyanka Palaka3, "**Dynamic Power Reduction in Digital VLSI Circuits Using Stacked LCNMOS**" published at: **International Journal of Advanced Research in Science and Technology**, Volume 7, Issue 1, 2018, pp. 757-760 .

7. S. Venkatesh, N. Sowmya, S. Krishna Veni "**Design of Low Power Multiplier Using Modified Reversible Logic Gate**" published at: **GVP Journal Of Science Technology And Management**, Volume 1, Issue 1-2017

8. G Amitha, M Chandra sekhar, D Santosh, Venkatesh S – **"An Area Efficient Reversible Multiplier Circuit Design By Using Low power Technique"** published at: **International Journal of Engineering Research and Applications (IJERA**) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 2, March -April 2013, pp.1819-1824.

9. BagadiMadhavi, G Kanchana, SeerapuVenkatesh – **Low Power and Area Efficient Design of VLSI Circuits** – published at: "**International Journal of Scientific and Research Publications (IJSRP)**, Volume 3, Issue 4, April 2013 Edition".

10. Venkatesh S, LaxmiPrasanna Rani M, " **Implementation Of Optimized Reconfigurable Built-In Self-Repair Scheme For Rams In Socs**" etal, **(IJCSIT) International Journal Of Computer Science And Information Technologies**, Vol. 3 (3) , 2012, 4443 – 4446.

Workshops attended:

- Participated in one-week international online FDP on **"Emerging Trends in Electronic Circuit Design, Signal Processing and Communication"** from 01-07-2024 to 08-07-2024. Organized by department of ECE, **koneru lakshmaiah education foundation, deemed to be university**, bachupally campus, hyderabad, telangana-500043.

- Successfully completed the 40-hour **Research Methodology** course organized at the **human resource development center, Andhra University** from 14-06-2023 t0 29-06-2023.

- Participated in Five days online workshop on **Full-Custom and Semi-Custom Design Flow using Cadence Tools** organized by **Department of ECE, GVP College of engineering(A) in association with Entuple Technologies Pvt.Ltd, Bengluru** from 25-07-2022 to 29-07-2022.

- Participated in Five days online workshop on **VLSI Design Using EDA Tools** organized by **GVP College of engineering, Visakhapatnam** from 18-04-2022 to 22-04-2022.

- Successfully Completed **Innovation Ambassador training (Advanced Level)** organized by **MoE's Innovation Cell & AICTE** from 30th June - 30th July 2021.

- Participated in Two Week FDP Course on **RISC-V VLSI Implementation Flow: RTL2GDS** organized by **Ministry of Electronics and Information Technology (MeitY**), Government of India from 27 March - 10 April, 2021.

- Participated in One Week FDP Course on **Low Power VLSI Design for Communication Systems and Networks** organized by **Dr. B R Ambedkar National Institute of Technology, Jalandhar** from 16-09-2020 to 20-09-2020.

- Participated in Three days FDP Course on **Antenna Design and Analysis using FEKO** organized by **Gayatri Vidya Parishad College for Degree and PG Courses (A)** from 22.06.2020 to 24.06.2020.

- Participated in One Week FDP Course on **Recent trends in VLSI** organized by **Gokaraju Rangaraju Institute of Engineering And Technology** from 02.06.2020 to 07.06.2020.

- Participated in Three days FDP Course on **Research Topics in VLSI and Industry Trends** organized by **GMRIT** from 29.05.2020 to 31.05.2020.

- Participated in One Week FDP Course on **IoT** organized by **Andhra Pradesh State Skill Development Corporation (APSSDC)** from 18.05.2020 to 30.05.2020.

- Participated in Two Day Training Program on **IIC Innovation Ambassador Training Program** at **MLR Institute of Technology** from 06.02.2020 to 07.02.2020.

- Participated in Two Day Workshop on **Learning Management System** at GVP **College for Degree and PG Courses (A)** from 30th April to 1st May 2019.

- Participated in Two Day Workshop on **Learning Management System** at GVP **College for Degree and PG Courses (A)** from 30th April to 1st May 2019.

- Participated in a three day workshop on **Custom Analog and Digital IC Design using Mentor EDA Tools** at **GVP college of engineering for women** from 27th to 29th September 2018

- Participated in a **Two-Week ISTE STTP on CMOS, Mixed Signal and Radio Frequency VLSI Design** conducted by **IIT Kharagpur** from 30th Jan 2017 to 4th Feb 2017.

- Worked as a co-convener in two day international conference **ICRIESHM-2016** at GVP College for degree and PG courses, school of engineering.

- Participated in a three day national workshop on **Analog and Digital Circuit Design using CADENCE** at GVP college of engineering

- Participated in a two day national workshop on VLSI & EDA TOOLS at JNTU, vizianagaram.

- Participated in a three day faculty development programme conducted by Dr. B.G. Barki, Retd. Professor of education NITTTR, Chennai at VITS Group of Institutions.

- Participated a three day faculty development programme on **Outcome-Based Engineering Education for Employability Enhancemen**t at VITS Group of Institutions.

- Participated in a Workshop on **LABVIEW Technologies** at MVGR College of engineering.

- Participated in **Digital Communication Faculty Development Program Conducted By APSCHE** in MVGRCollege of engineering.

- Participated in **WOLTEC (Workshop on Latest Technologies in Electronics and Communications)** at MVGRCollege of engineering.

- Participated in **Xilinx** workshop at GVP College of engineering.

Professional Bodies Membership:

- Member of International Association of Engineers with Id: 232386
- Member of IFERP with Id: PMIN40392785

Achievements:

- Qualified for Assistant Professor in UGC-NET June, 2019.
- Ratified as Assistant Professor by Andhra University.
- Qualified in GATE-2016.
- Qualified in GATE-2013.
- Received prize in B.Tech for being topper in academics.

Subjects Thought:

1. VLSI
2. Micro Electronics
3. Electronic Devices and Circuits
4. Switching Theory and Logic Design
5. Digital system Design Through Verilog
6. VLSI Design Verification & Testing
7. Pulse and Digital Circuits
8. Digital Communication
9. Information Theory and Coding
10. Basic Electronics Engineering
11. Micro Wave Engineering

Personal Details:

Father's Name	:	S. Krishnarao
Date of Birth	:	10th June 1988
Marital Status	:	Married
Religion	:	Hindu
Nationality	:	Indian
Sex	:	male
Languages Known	:	English, Telugu

DECLARATION

I hereby declare that all statements made above are true, complete and correct to the best of my knowledge and belief.

Date:

Place: Visakhapatnam. S.Venkatesh