GAYATRI VIDYA PARISHAD COLLEGE FOR DEGREE AND P.G. COURSES (A)
RUSHIKONDA, VISAKHAPATNAM 530045.
(Approved by A.I.C.T.E | Affiliated to Andhra Univeristy | An ISO 9001:2015 Certified Institute)
ENGINEERING AND TECHNOLOGY PROGRAM
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

LIST OF GUEST LECTURES CONDUCTED

S. NO.	ACADEMIC YEAR	DATE OF GUEST LECTURE	DETAILS OF THE RESOURCE PERSON	TOPIC
1	2020-21	25.01.2021	Avinash Yadlapati, Senior Director –Engineering, Mirafra Technologies	An Overview of VLSI Design and Opportunities
2	2020-21	04.07.2020	Sri. G. Anantram, Consultant and Content, Developer/Editor for Start-Ups	Innovation to Entrepreneurship ... A journey of excitement

H.O.D-ECE

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LIST OF WORKSHOPS / CONFERENCES CONDUCTED

S. NO.	ACADEMIC YEAR	DATE OF WORKSHOP	DETAILS OF THE RESOURCE PERSON	DETAILS OF THE WORKSHOP
1	2020-21	22-06-2020 to 24-06-2020	Summet Pillai, Altair FEKO Solutions	Online FDP on Antenna Design and Analysis using FEKO
2	2020-21	02-11-2020 to 06-11-2020	Prof P.Rajesh Kumar, HOD-ECE, AUCOE(A)	AICTE ATAL SPONSORED FACULTY DEVELOPMENT PROGRAM ON ADVANCES IN SENSOR TECHNOLOGY
			Prof Hardik J. Pandya, Division of EECS, IISc Bangalore	
			Sujatha, Centre of Excellence in MEMs Microfluidics(CEMM), Rajalakshmi Engineering College, Chennai	
			Dr.G.Venkat Reddy, Director RCI Lab, Scientist-H, DRDO, Hyderabad	
			Mr. K.Bapuji, CEO, Appleton Innovations	
			Mr. Kamal Kumar, Staff Engineer, Savari Systems, Bengaluru	
			Bandana Rai, Founder and Chief Mentor at AnanyaTEC Training Education and Consulting Services	
			Dr. P.Srihari, Asst. Professor, NITK	
			Mr. D. Ramesh, Red Silicon Labs	
			Nitin S Kale CTO, Nanosniff Technologies Pvt Ltd, IIT Bombay	
3	2020-21	28-12-2020 to 30-12-2020	Mr J Prem Kumar, Product Manager for Mathworks Products, Capricot Technologies Pvt. Ltd.	Online Workshop on Applications of Signal and Image Processing using MATLAB

H.O.D-ECE

REPORT

"ADVANCES IN SENSOR TECHNOLOGY (AST-2020)"

Date: 02nd November 2020 - 06th November 2020,

Institute Name: GAYATRI VIDYA PARISHAD COLLEGE FOR DEGREE AND PG COURSES (A),

ENGINEERING AND TECHNOLOGY PROGRAM

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

“ADVANCES IN SENSOR TECHNOLOGY (AST-2020)”

The Department of Electronics and Communication Engineering organized a Five-day Faculty Development Programme (FDP) on “Advances in Sensor Technology (AST-2020)” under ATAL Sponsored FDP, 103 participants all over the country registered for this FDP, out of which 74 participants participated in all the FDP sessions. The feedback from the participants is very good and the content delivered by all the resource persons is very good.

The speakers for the 5-day FDP on “**“ADVANCES IN SENSOR TECHNOLOGY (AST-2020)”** were:

Prof. P. Rajesh Kumar, HOD -ECE, AUCOE.

Dr. P. Rajesh Kumar is presently Professor and Head of the department of Electronics and Communication Engineering, Andhra University College of Engineering (Autonomous), Visakhapatnam. He graduated from CBIT affiliated to Osmania University, Hyderabad. He Received his ME and Ph.D from Andhra University, Visakhapatnam. He has 22 years of teaching experience and guided many students for their thesis work. He has published more than 100 research papers in various national and International Journals/Conferences. Presently he is guiding 18 research scholars. Twenty research scholars received their Ph.D. degree under his guidance and three scholars submitted their Ph.D. thesis and awaiting for the award. He is member of IEEE, IETE, ISTE, SEMCE (I) and Instrument Society of India. He was also convener for INCEMIC 2015. Presently he is hon'ry Secretary for IETE Visakhapatnam Centre. Earlier he was hon'ry Treasurer and Vice-Chairman for IETE Visakhapatnam Centre. His research interests are Radar Signal Processing, Image Processing and Bio-medical Signal Processing.

Prof Hardik J. Pandya, Division of EECS, IIS, Bangalore

Professor Hardik J. Pandya joined the Department of Electronic Systems Engineering, Division of EECS, Indian Institute of Science, Bangalore in January 2017. Dr. Pandya heads three laboratories in ESE focused on developing a new class of biomedical devices and technologies. Before joining IISc, he worked as a postdoctoral scientist in the Department of Mechanical Engineering, Maryland Robotics Center, University of Maryland, College Park (2012-2016) and in the Department of Medicine, Brigham and Women’s Hospital–Harvard Medical School (2016-2017). He obtained his Ph.D. in Microelectronics Technology from the Indian Institute of Technology Delhi (2013). His current research focuses on minimally invasive and non-invasive technologies with an emphasis on but not limited to cancer diagnosis (brain, breast, head and neck), e-nose (diabetes, breast cancer screening), Neuro protective Therapies for Acute Stroke and Epilepsy.

Dr. L. Sujatha, Professor and HOD, REC COLLEGE

Dr. L. Sujatha, Head, Centre of Excellence in MEMS & Microfluidics (CEMM) and Professor in the Department of Electronics & Communication Engineering, Rajalakshmi Engineering College (REC), Chennai has 30 years of experience in teaching and research. Graduating with an A.M.I.E. in Electronics & Communication Engineering from Institution of Engineers (INDIA) in 1991, she obtained her M.E. (Applied Electronics) from Bharathiar University in 1996. She has done her PhD and Post-Doctoral Research in the field of Micro Electro Mechanical Systems (MEMS) at Indian Institute of Technology Madras. She is a recognized supervisor under Anna University and guided 3 research scholars for their PhD degree. She has published two book chapters, 40 journal papers in refereed international journals, more than 60 International Conferences. She had received a "Best Woman Engineer" award from Pondicherry Engineering College in the year 2007 and received "Dr. A.P.J. Abdul Kalam Award for Innovative Research" by Society for Engineering Education Enrichment (SEEE) in the year 2017.

Dr. G. Venkat Reddy, Scientist H, RCI (Research Centre Imarat), Hyderabad

He is working as Scientist H, RCI (Research Centre Imarat), Hyderabad. Graduated his BE (ECE) from University College of Engineering, Osmania University and Post-graduation (M.Tech.) from Indian Institute of Technology Kharagpur.

Working in the field of development of hardware and software for Avionics for unmanned and manned Aircraft and Aerospace vehicles for more than three decades.

Mr. K.Bapuji, Technical Trainer on Internet of Things

He is a technical Trainer on Internet of Things (IoT). He worked in KVK Energy Infrastructure private Limited, Satyams Byrraju Foundation as Project Head for 6 years. He worked on an innovative Project Ashwini wireless long distance network in collaboration with IIT Kanpur computer science department. He is having 10+ years' experience in Internet of Things Research and Training. He is founder of and director of Appleton Innovations. He designed and developed Internet of Things Boards and kits with trademark "**HUEBITS".**

He designed and developed software package for AHP using **MATLAB and SCILAB** and can be accessed at IIT Bombay site:
https://www.ee.iitb.ac.in/~belur/AHP/

Mr. Kamal Kumar, Staff Engineer Savari Inc

He is a technical Trainer on C, C++, Python, Linux system programming and IoT devices. He worked in Huawei Technologies as Technical Lead from April 2011 to July 2017. Having 10+ years' experience in Internet of Things and software development and in Internet of Things Training. He is currently working as a Staff Engineer at Savari Inc.

Professional Experience as a Trainer

Gave more than 20 Training programs on IoT, Python at India's best Institute like Great Lakes Learning.

Mrs. Bandana Rai, Founder and Chief Mentor at AnanyaTEC Training Education

Founder and Chief Mentor at AnanyaTEC Training Education and Consulting Services, with 22 plus years of exposure to service and allied sector, her skill sets primarily include Identifying and Practicing Innovative Learning Solutions aligned with Organizational Strategic Talent Management guidelines for all related stakeholders.

Dr. P. Srihari, Founder of Sri Shasha Prayathi Technologies PVT LTD

He is graduated B.Tech in ECE from Sri Venkateswara University, he obtained master's degree from University of Plymouth, England, UK and PhD from Andhra University in the tears 2000, 2002 and 2012 respectively.He is senior member of IEEE, ACM and a fellow of IETE. His research interests are radar systems, radar signal processing, radar target tracking and navigation systems. He is also founder of Sri Shasha Prayathi Technologies PVT LTD. Incubated by National institute of Technology Karnataka Science and Technology Entrepreneurship Park (NITK-STEP), Surathkal. He has guided two PhDs in this area and worked on radar waveform design. He is engaged with multiple government organizations (specifically defence) like RCI, Hyderabad, LRDE, Bangalore and Central research Laboratory (CRL)-Bharat Electronic Limited (BEL), Bangalore and Asymmetric Technologies Laboratory (ASTL), Kolkata in the area of radar signal processing and radar target tracking.

Mr. D. Ramesh, Founder of and Director of Redsilicon Labs

He obtained M.Tech from JNTU Kakinada.He is a technical Trainer on Embedded Systems. He worked in Redpine signals, Akrivia Automation as a R&D Engineer. He designed and developed IoT based products. He is having 5+ years' experience in Internet of Things product development and Training. He is founder of and director of redsilicon labs. He trained corporate employees, students on embedded systems design and IoT.

Prof.Nitin S Kale, Nano Sniff Technologies

Nitin S. Kale obtained his M. Tech from VNIT Nagpur in 1999, and his Ph. D. from the Electrical Engineering Department at IIT Bombay in 2007. During 2007 – 2008, he worked as a Principal Engineer at Taiwan Semiconductor Manufacturing Company, on the 32-nm High-K Metal Gate project. In 2009 he joined the IIT Bombay Nano manufacturing Facility as its Manager. In this role he was responsible for the day to day operations and management of the Rs.200 Crore IIT Bombay Nanofabrication Facility. Since June 2011, he is working with Nano Sniff Technologies, which is a technology start-up company incubated at IIT Bombay. He is responsible for the R&D in the area of fabricating micro cantilever sensors, micro heaters; and developing instruments for detecting explosives, proteins and antibodies, using micro cantilever based measurements.

He has developed **5 Products**, which include: 1. Instruments: (i) Omni cant; (ii) Sensimer; 2. MEMS Devices: (i) Piezo resistive Micro cantilevers; (ii) Micro heaters. 3. Hotwire-CVD Cluster Tool for Depositing Thin Films of Polysilicon, Silicon Nitride etc. He has demonstrated the **Proof of Concept of detecting Explosives** using MEMS Micro heaters & High-Speed & High-Sensitivity Electronics. He has also demonstrated the **Proof of Concept of detecting Cardiac Proteins (hFAbP, Myoglobin etc)** using Piezo resistive Micro cantilevers, ultrasensitive electronics, & a Custom-made Liquid-Cell.

ATAL FDP **on "ADVANCES IN SENSOR TECHNOLOGY (AST-2020)"**

FDP Schedule is as follows:

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(Program Accredited by NBA)

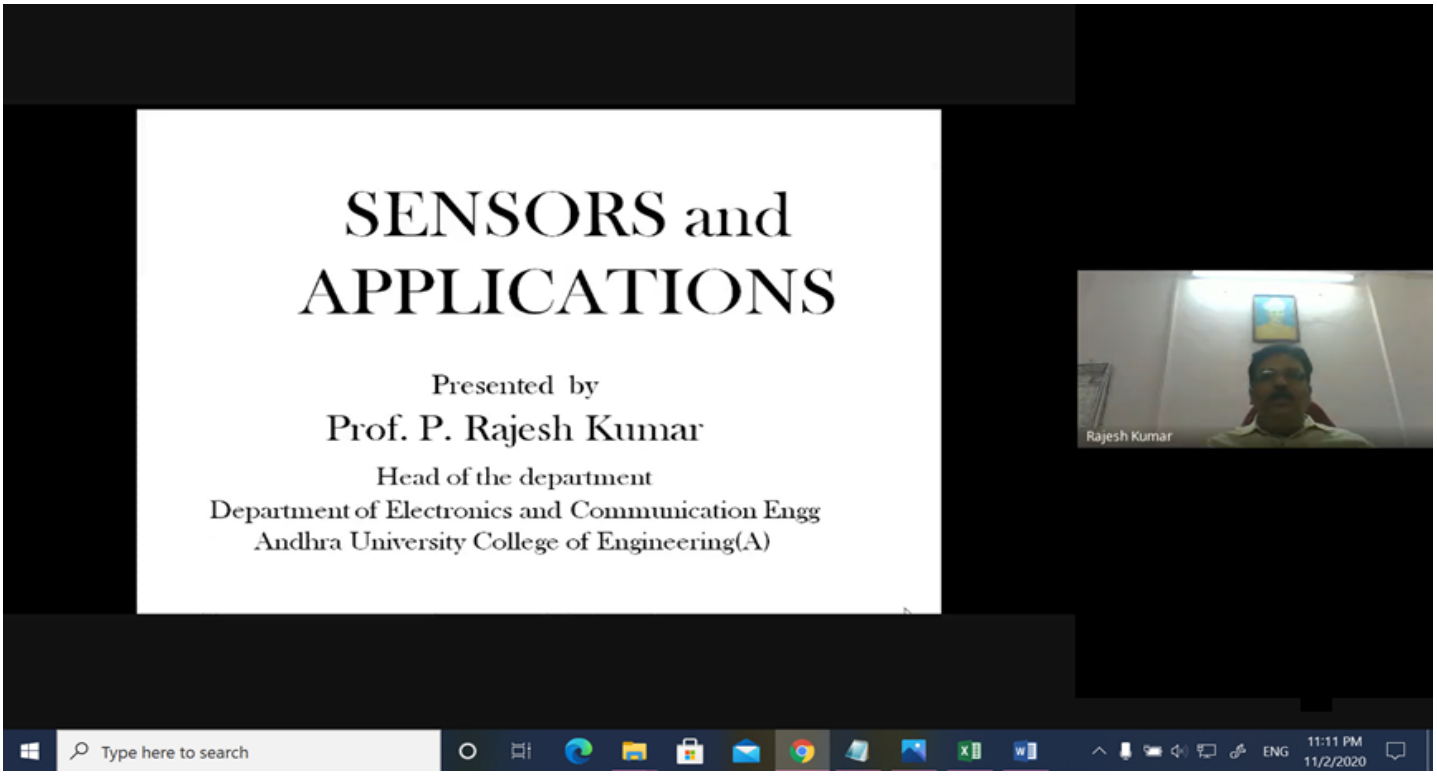
SCHEDULE OF AICTE ATAL SPONSORED FACULTY DEVELOPMENT PROGRAM ON
"ADVANCES IN SENSOR TECHNOLOGY" (02nd November 2020 - 06th November 2020)

Date & Time	Forenoon Session				Afternoon Session
	10:00 AM to 11:30 AM	Break	12:00 PM to 1:30 PM	Lunch Break	2:30 PM to 4:00 PM
Monday 02.11.2020	Key note address by Prof P.Rajesh Kumar HOD-ECE, AUCOE(A)		"Smart Sensors" Prof Hardik J. Pandya Division of EECS, IISc Bangalore		"Microfluidic Technology for Biosensors" Prof. L. Sujatha, Centre of Excellence in MEMs Microfluidics(CEMM), Rajalakshmi Engineering College, Chennai
Session link	https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj
Tuesday 03.11.2020	"Inertial Navigation Sensors and Interfaces" Dr.G.Venkat Reddy, Director RCI Lab, Scientist-H, DRDO, Hyderabad		"Smart Sensors" Prof Hardik J. Pandya Division of EECS, IISc Bangalore		"MEMS Accelerometers" Prof. L. Sujatha, Centre of Excellence in MEMs Microfluidics(CEMM), Rajalakshmi Engineering College, Chennai
Session link	https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj
Wednesday 04.11.2020	"Internet of Things (IoT)" Mr. K.Bapuji CEO, Appleton Innovations		"Internet of Vehicles" Mr. Kamal Kumar, Staff Engineer, Savari Systems, Bengaluru		"Emotional Competencies and Stress Management" Bandana Rai Founder and Chief Mentor at AnanyaTEC Training Education and Consulting Services
Session link	https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj
Thursday 05.11.2020	"Signal Processing for RF Sensors" Dr. P.Srihari Asst. Professor, NITK		"Internet of Things (IoT)" Mr. K.Bapuji CEO, Appleton Innovations		"Embedded Programming for Smart Sensors" Mr. D. Ramesh Red Silicon Labs
Session link	https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj
Friday 06.11.2020	"MEMs Sensors" Nitin S Kale CTO, Nanosniff Technologies Pvt Ltd, IIT Bombay		"MEMs Sensors" Nitin S Kale CTO, Nanosniff Technologies Pvt Ltd, IIT Bombay		Test, Feedback and Validictory
Session link	https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj		https://meet.google.com/yfh-hxmz-fjj

Mr. S.Sandeep
FDP Co-Cordinator

Dr. S. Krishna Veni
FDP Cordinator

A common inaugural was launched for 39 ATAL FDPs by the distinguished persons from AICTE. Followed by which we had launched our FDP by the gracious presence of Prof P.Rajesh Kumar, Principal Prof S.Rajanai madam, Vice principal Prof D.Saritha madam. All the members on this occasion, have motivated the department for organizing such FDP and suggested the participants to acquire the maximum benefit. And some screenshots of the inaugural function are as below. Director ATAL, Prof. Ravindra Soni addressed the participants about online FDP and various initiatives by ATAL Academy. Prof Kakde talked about IIIT Roles and Responsibility in technical education. Prof. Poonia Sir, discussed about various AICTE initiatives.



The list of participants was:-

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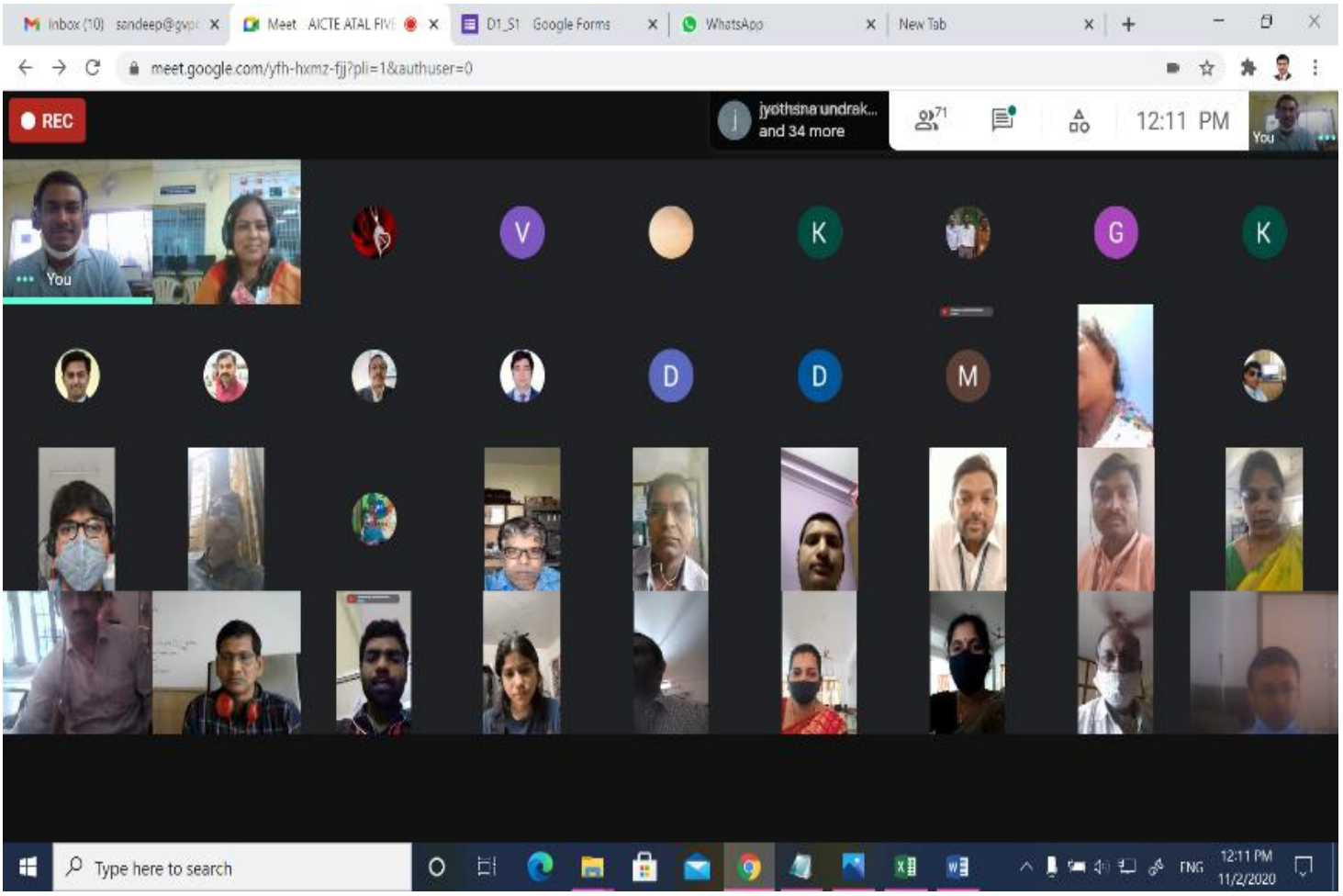
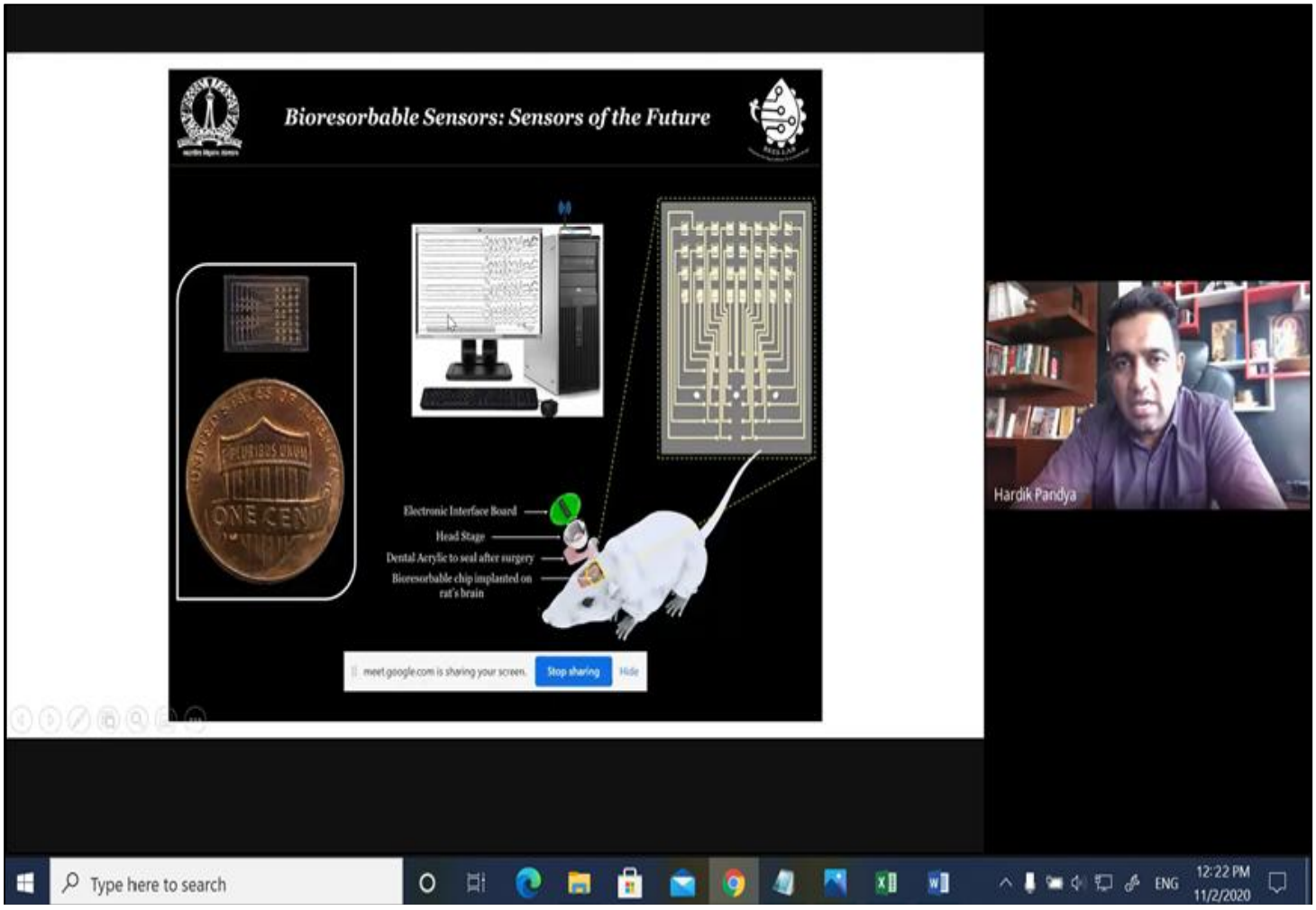
102	Mr. Sajid Karim Shaikh	sajidshaikh1433@gmail.com	9987350998
103	Mrs. Rubina Shaikh	srubinabee@mes.ac.in	9987863209

The screenshots of the participants taken on the closing are:-

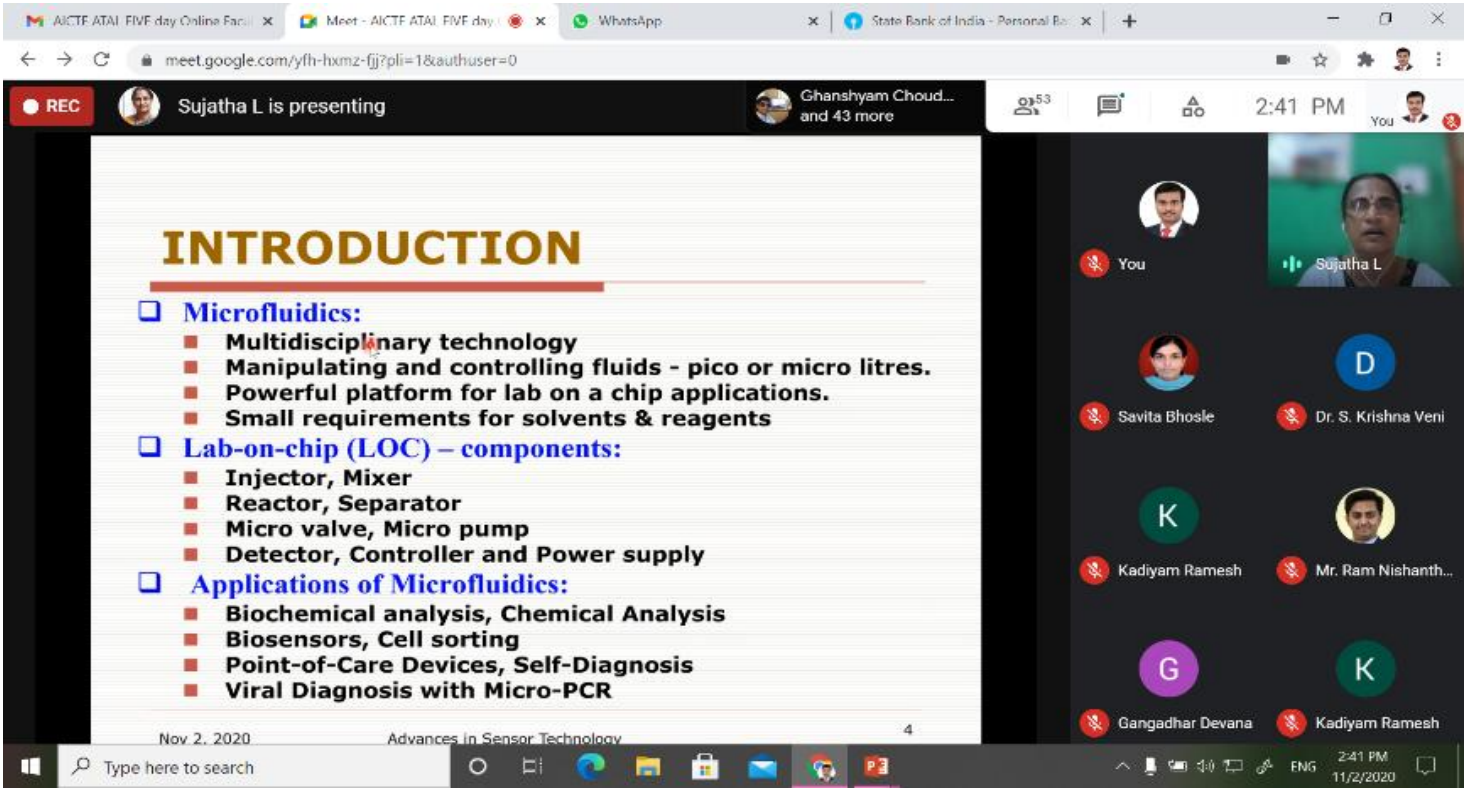
Day 1 Session 1

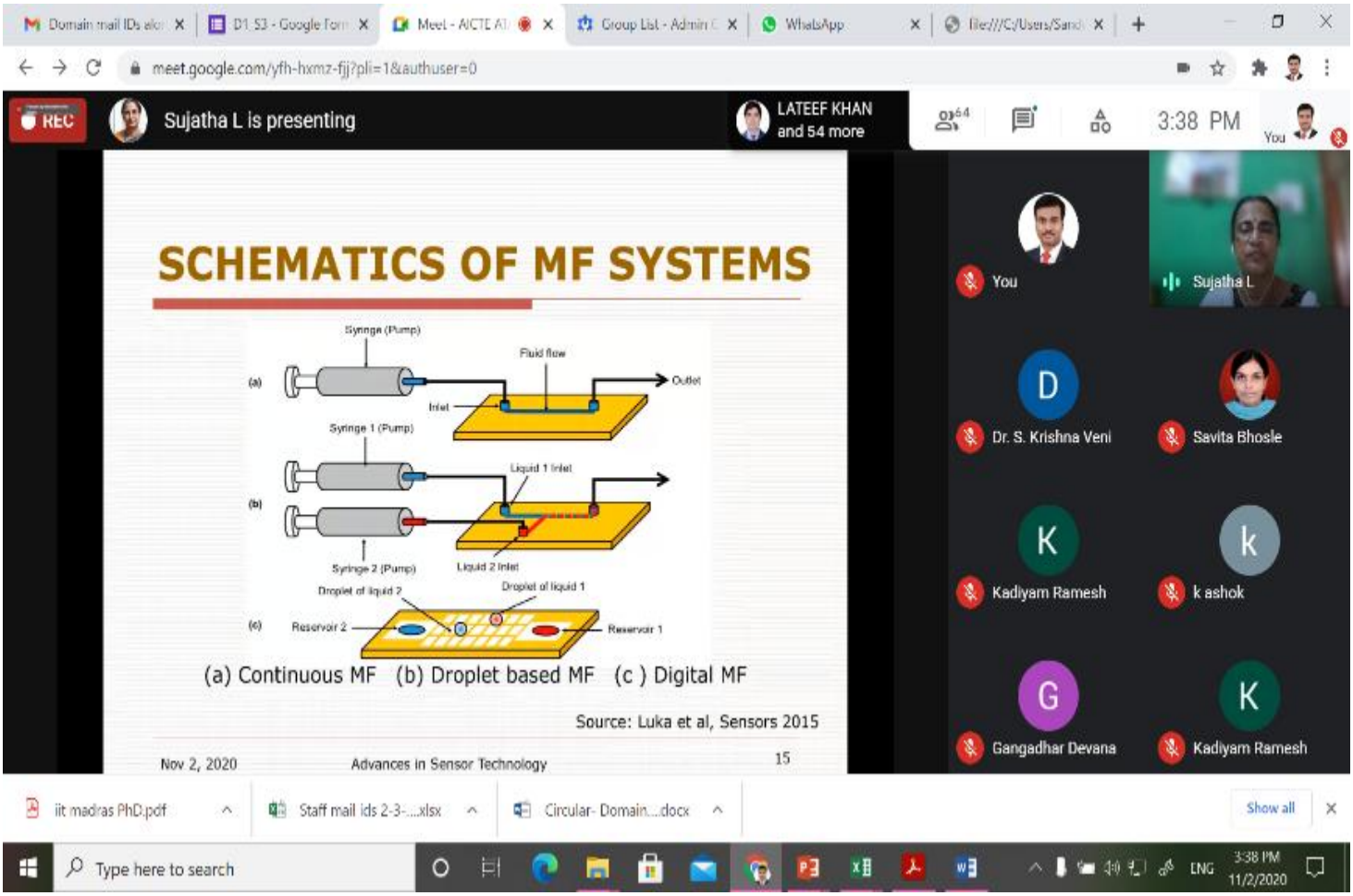


Day 1 Session 2

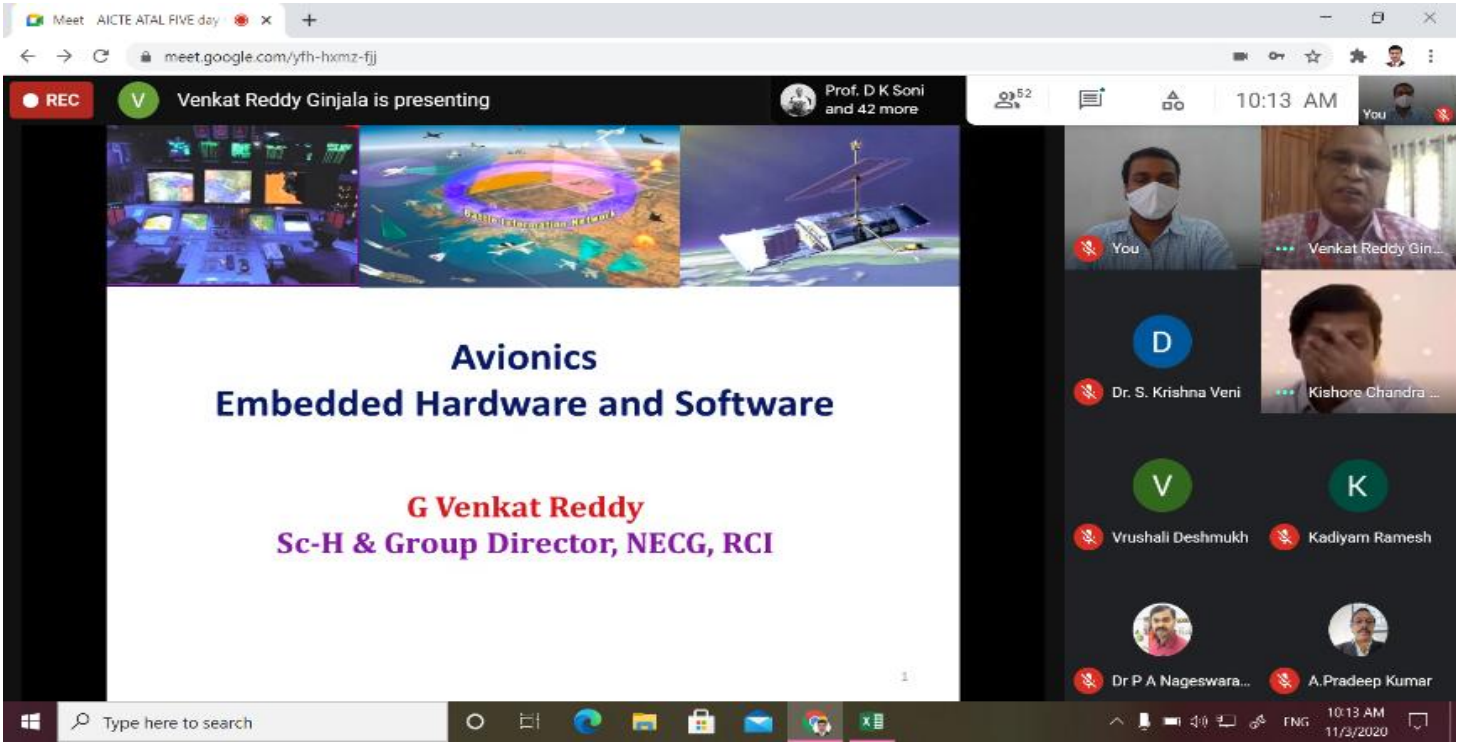


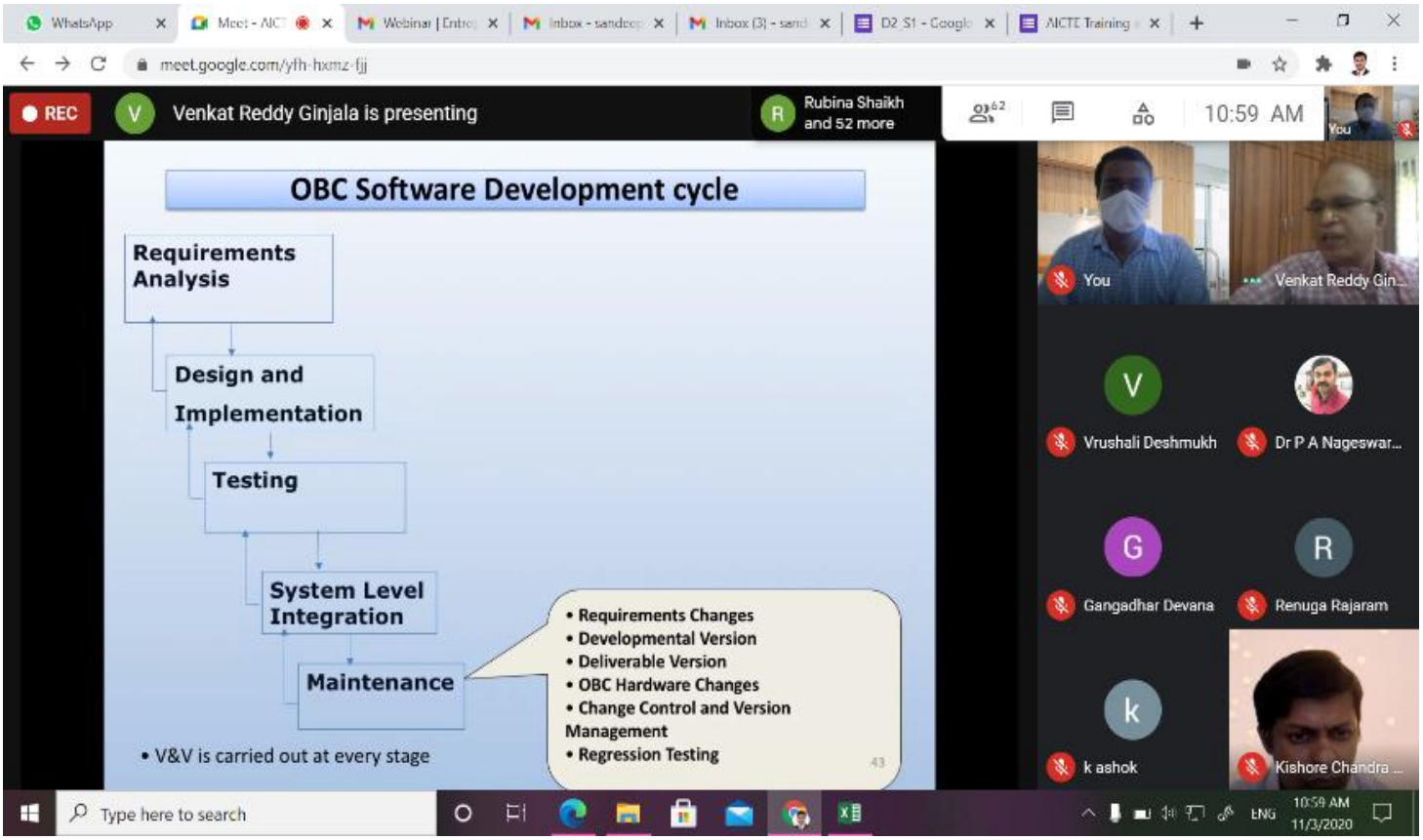
Day 1 Session 3

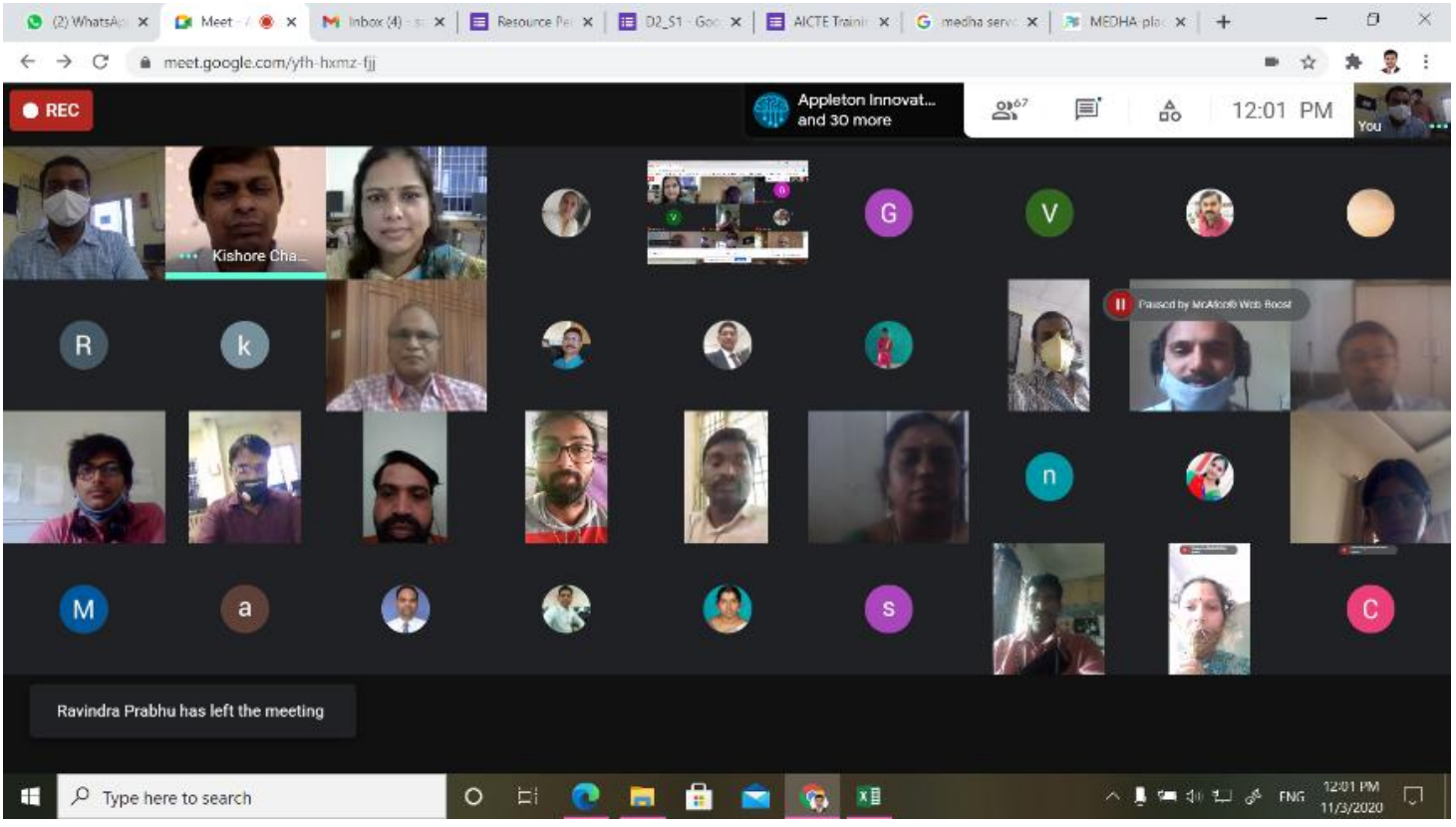




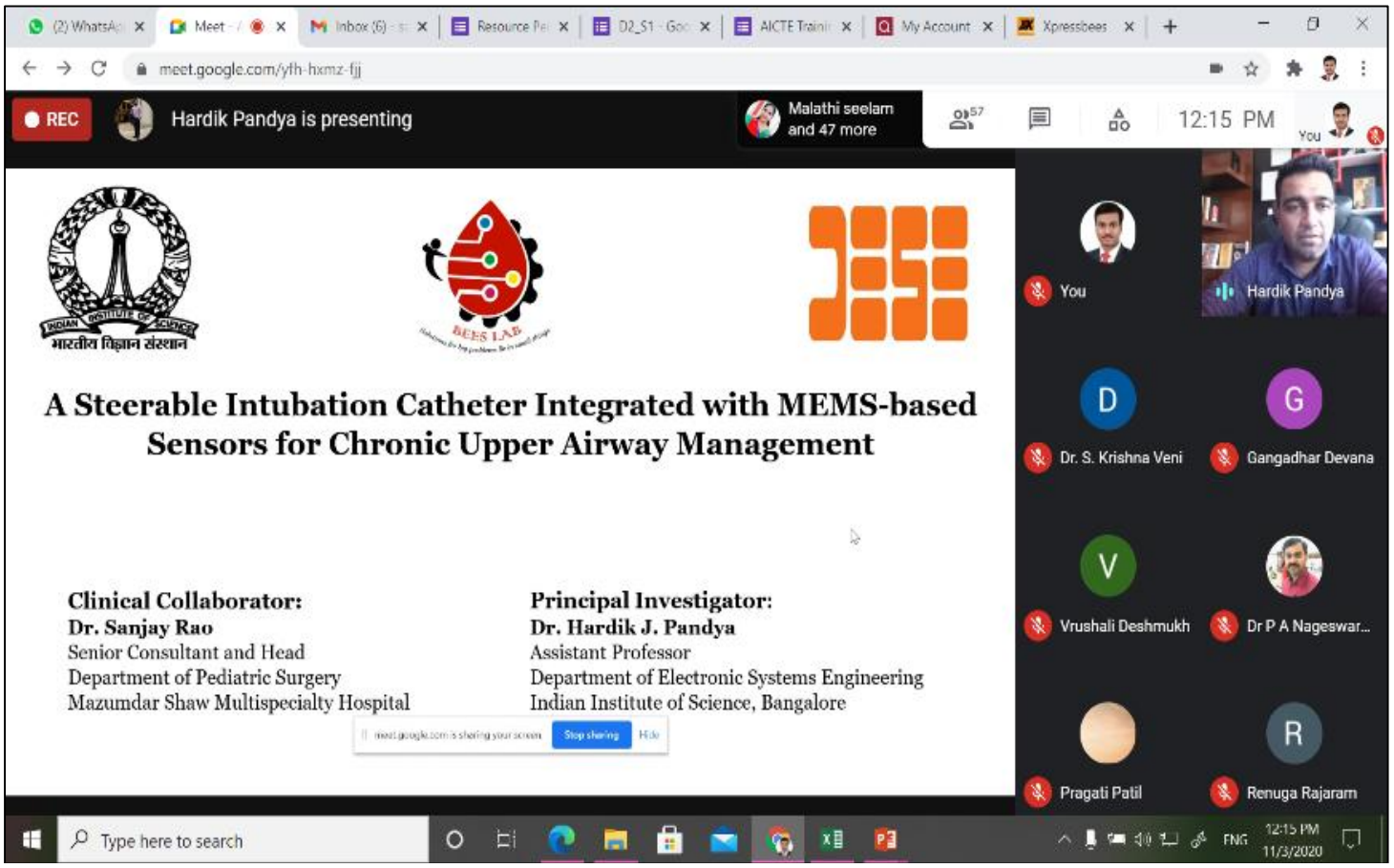
Day 2 Session 1

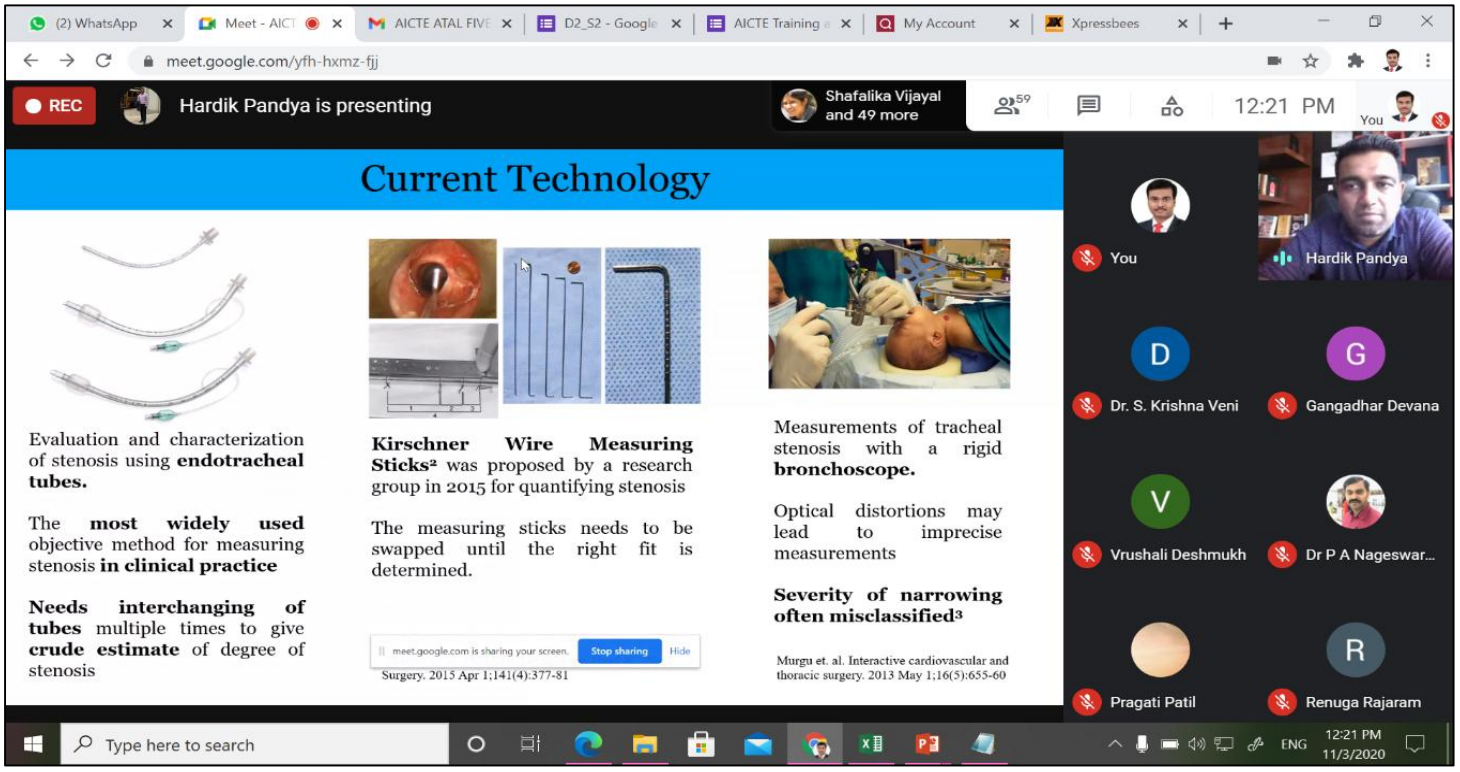


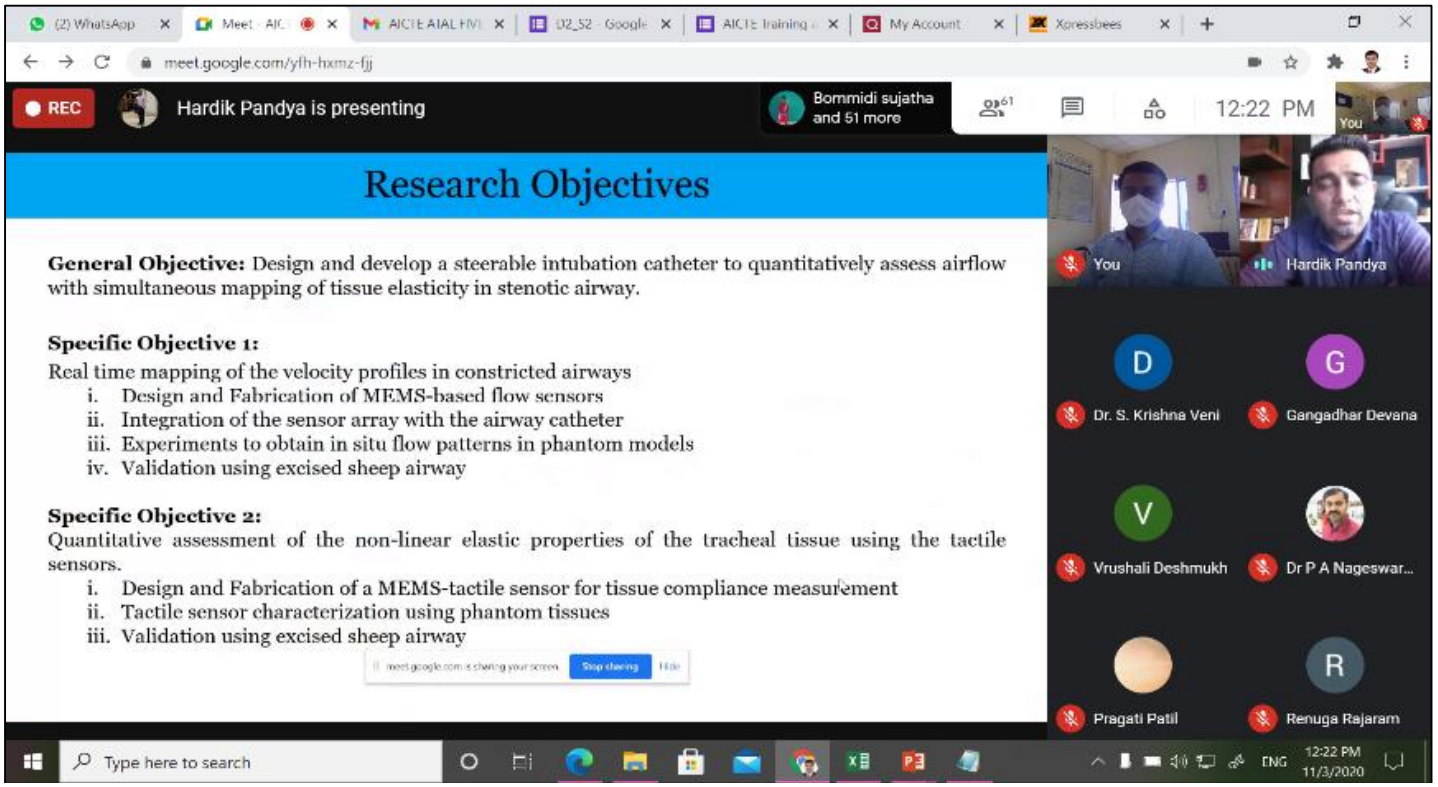

REC
Venkat Reddy Ginjala is presenting
Rubina Shaikh and 52 more
10:59 AM
OBC Software Development cycle
Requirements Analysis
Design and Implementation
Testing
System Level Integration
Maintenance
• Requirements Changes
• Developmental Version
• Deliverable Version
• OBC Hardware Changes
• Change Control and Version Management
• Regression Testing
• V&V is carried out at every stage
You
Venkat Reddy Gin...
Vrushali Deshmukh
Dr P A Nageswar...
Gangadhar Devana
Renuga Rajaram
k ashok
Kishore Chandra ...
Type here to search

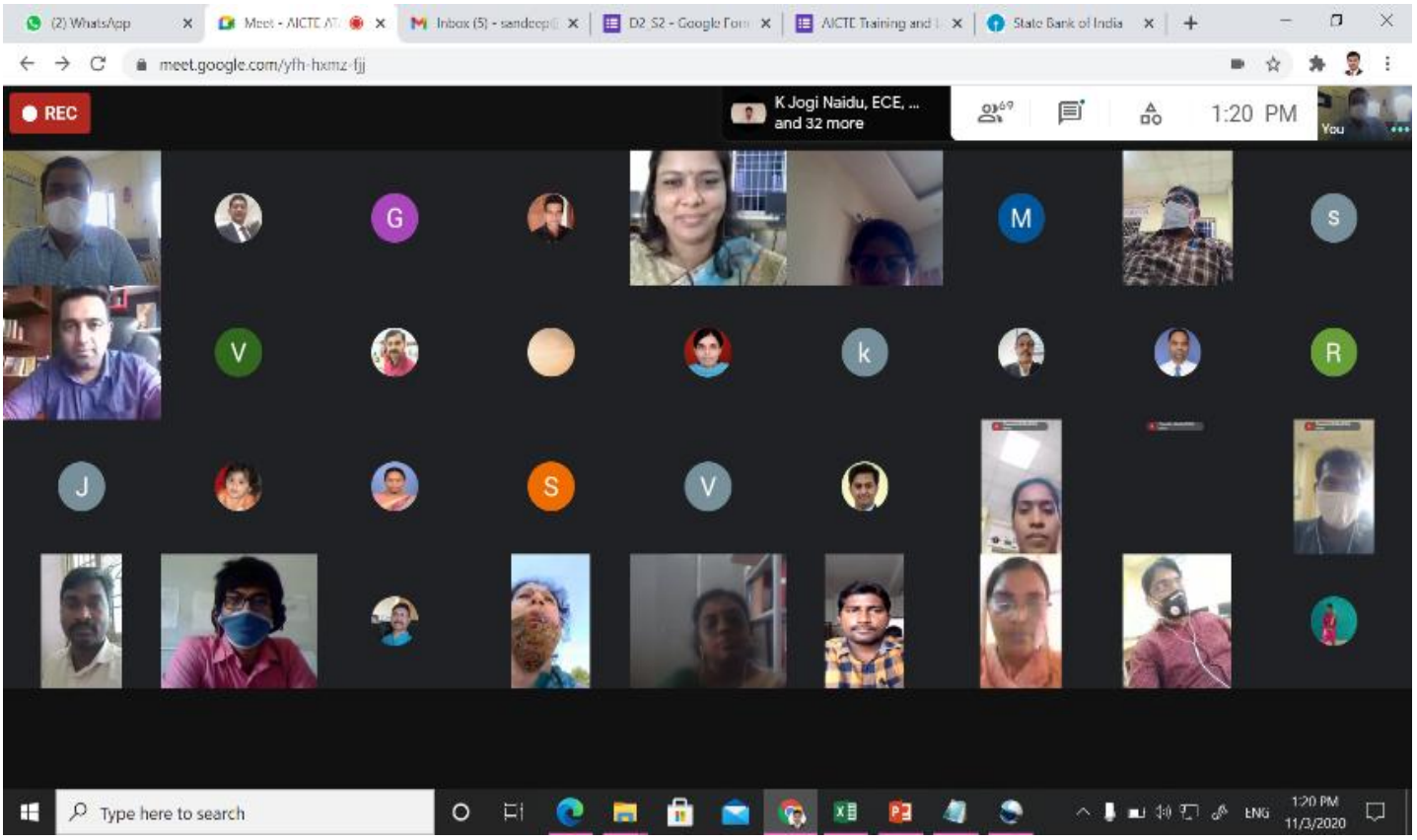

REC
Appleton Innovat... and 30 more
12:01 PM
You
Kishore Cha...
Ravindra Prabhu has left the meeting
Type here to search

Day 2 Session 2

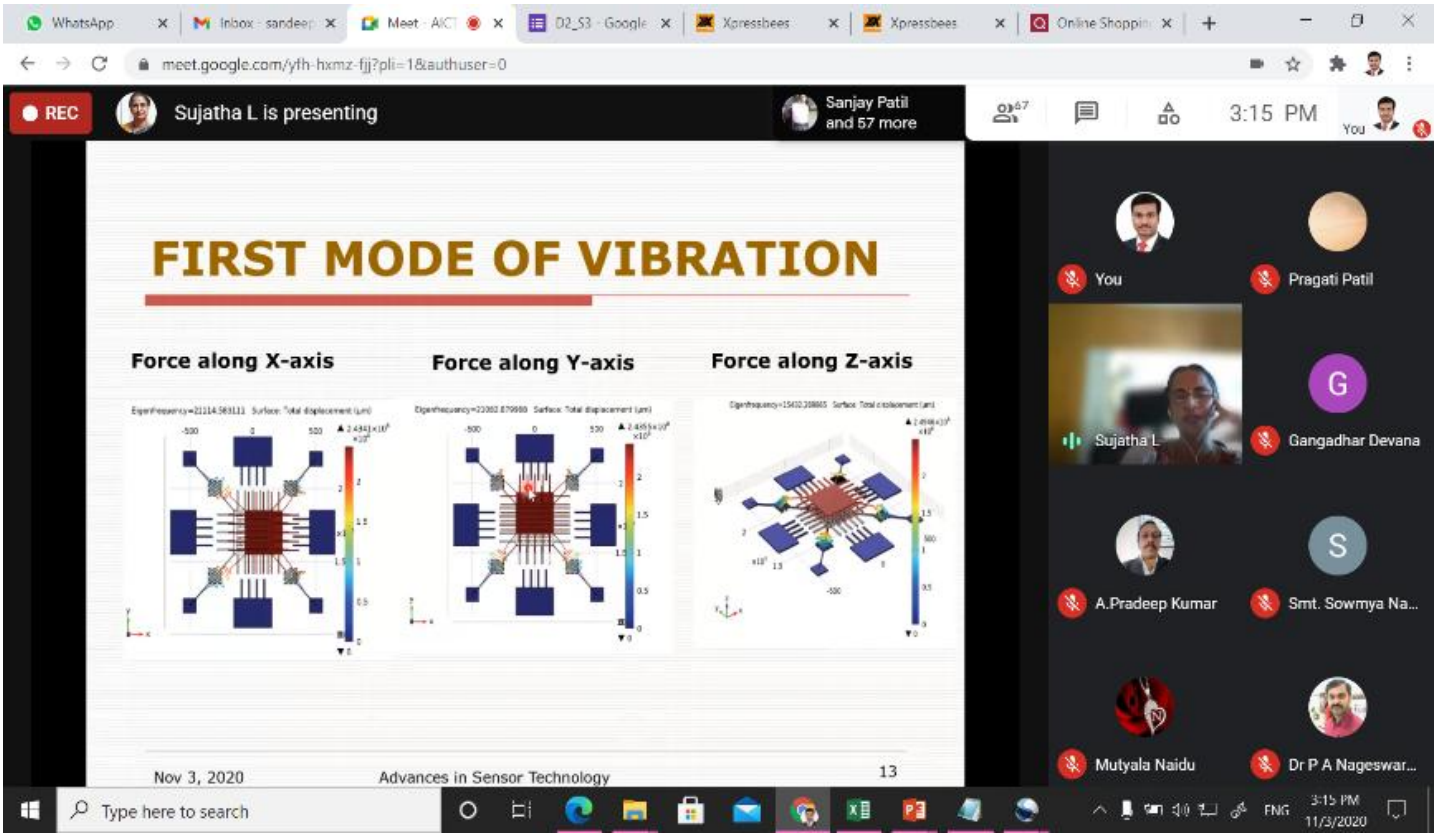


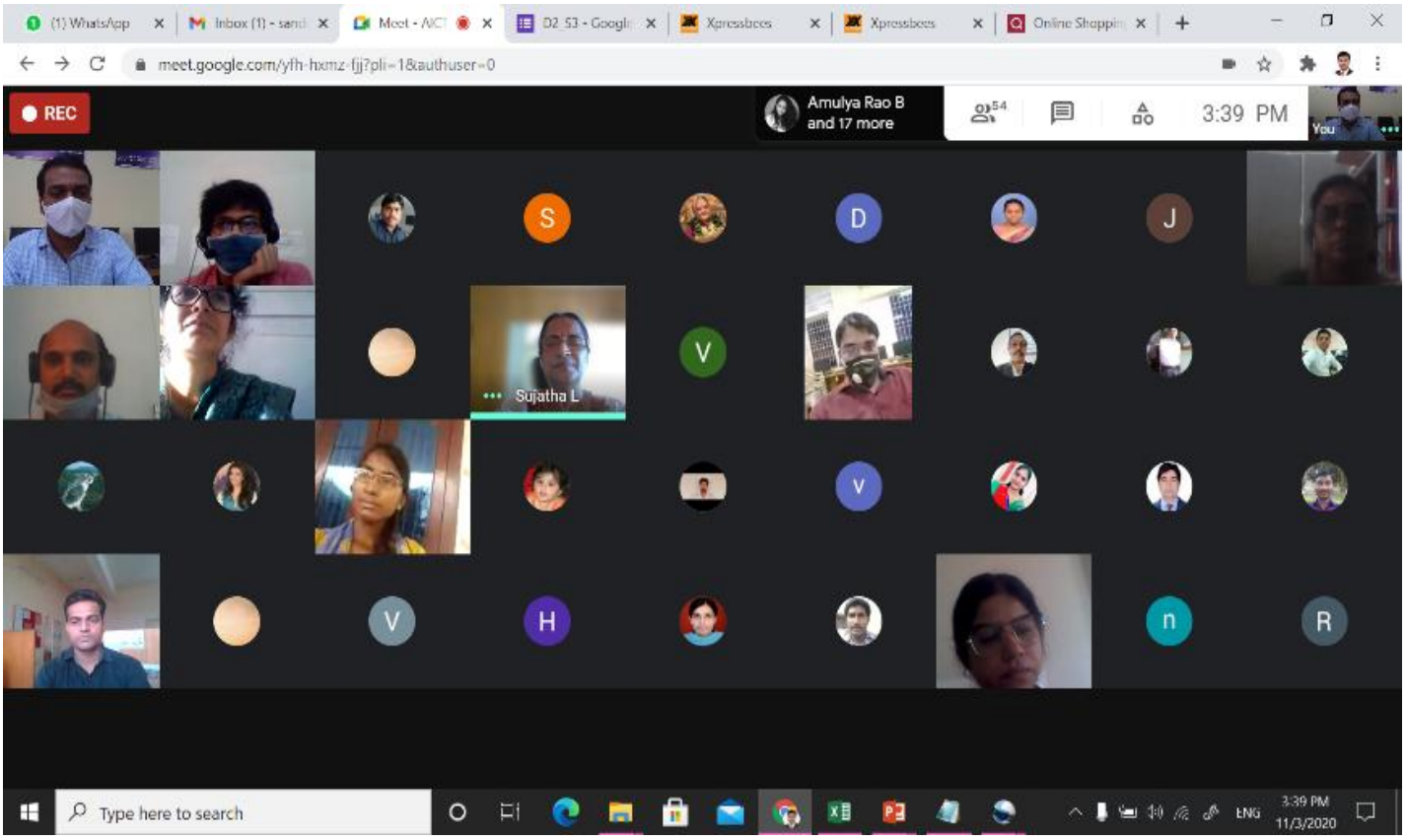



meet.google.com/yfh-hxmz-fjj
REC
Hardik Pandya is presenting
Bommidi sujatha and 51 more
12:22 PM
You
Research Objectives
General Objective: Design and develop a steerable intubation catheter to quantitatively assess airflow with simultaneous mapping of tissue elasticity in stenotic airway.
Specific Objective 1:
Real time mapping of the velocity profiles in constricted airways
i. Design and Fabrication of MEMS-based flow sensors
ii. Integration of the sensor array with the airway catheter
iii. Experiments to obtain in situ flow patterns in phantom models
iv. Validation using excised sheep airway
Specific Objective 2:
Quantitative assessment of the non-linear elastic properties of the tracheal tissue using the tactile sensors.
i. Design and Fabrication of a MEMS-tactile sensor for tissue compliance measurement
ii. Tactile sensor characterization using phantom tissues
iii. Validation using excised sheep airway
You
Hardik Pandya
Dr. S. Krishna Veni
Gangadhar Devana
Vrushali Deshmukh
Dr P A Nageswar...
Pragati Patil
Renuga Rajaram
Type here to search
ENG
12:22 PM
11/3/2020

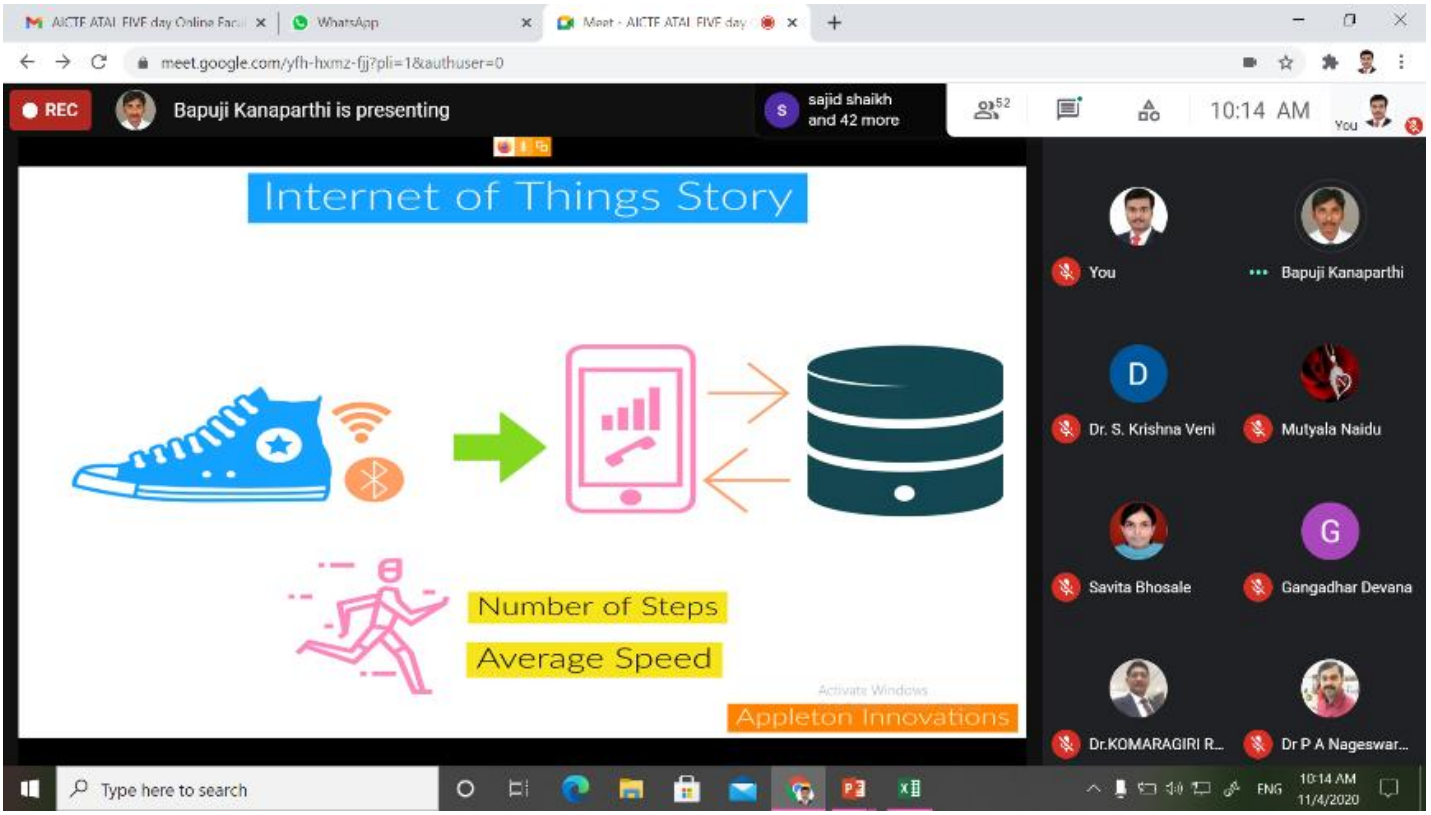

meet.google.com/yfh-hxmz-fjj
REC
K Jogi Naidu, ECE, ... and 32 more
1:20 PM
You
Type here to search
ENG
1:20 PM
11/3/2020

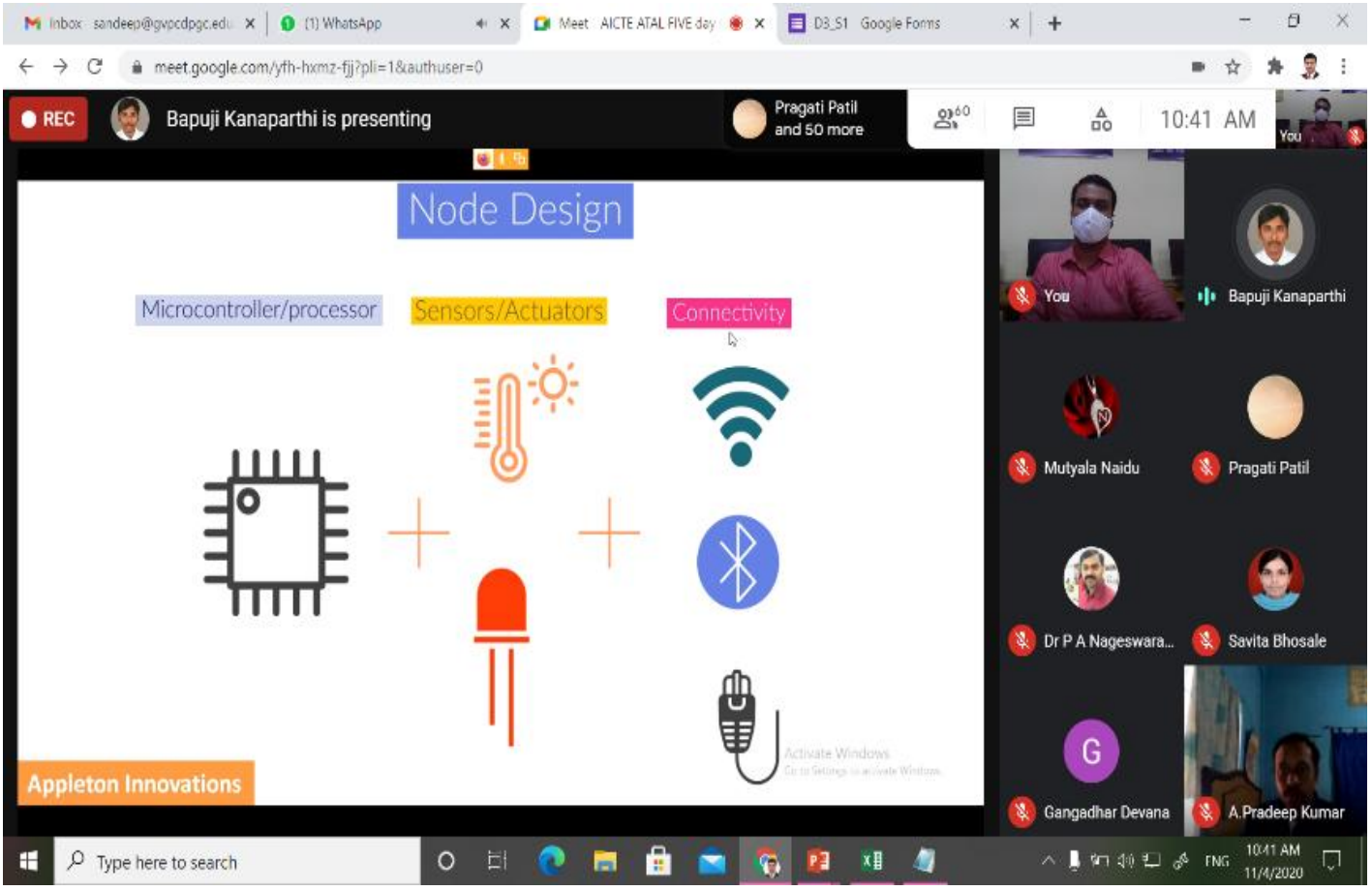
Day 2 Session 3

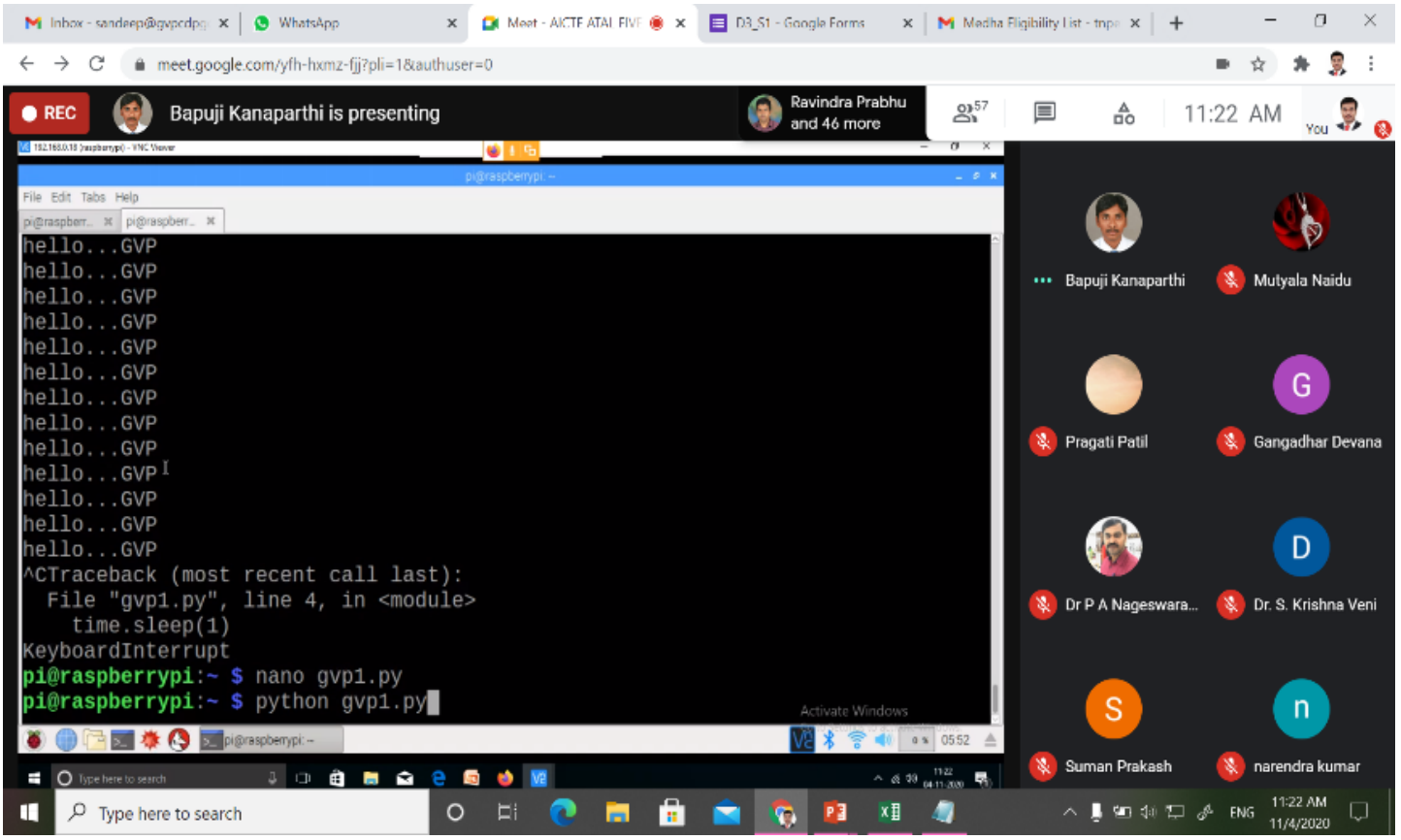


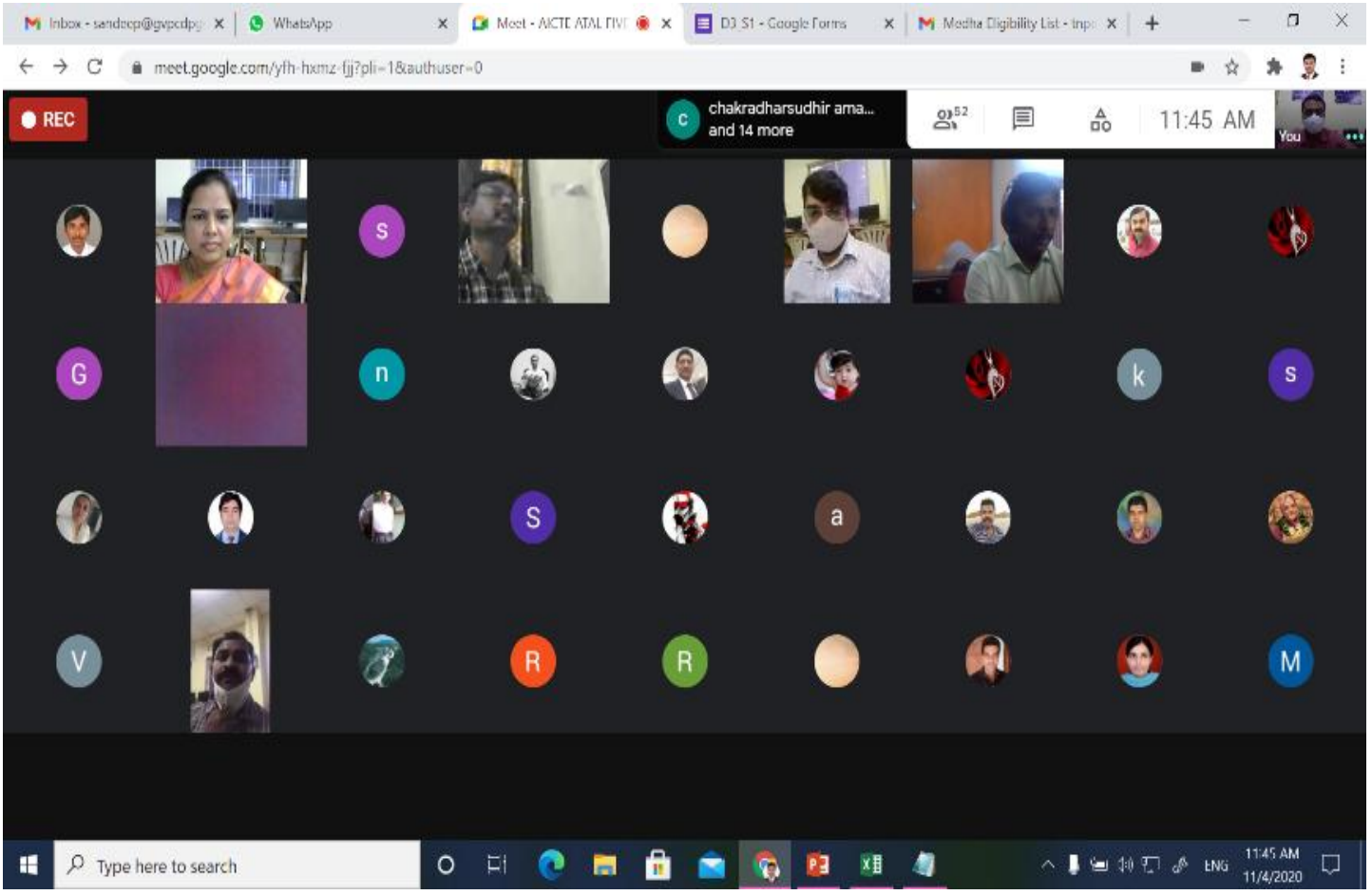


Day 3 Session 1

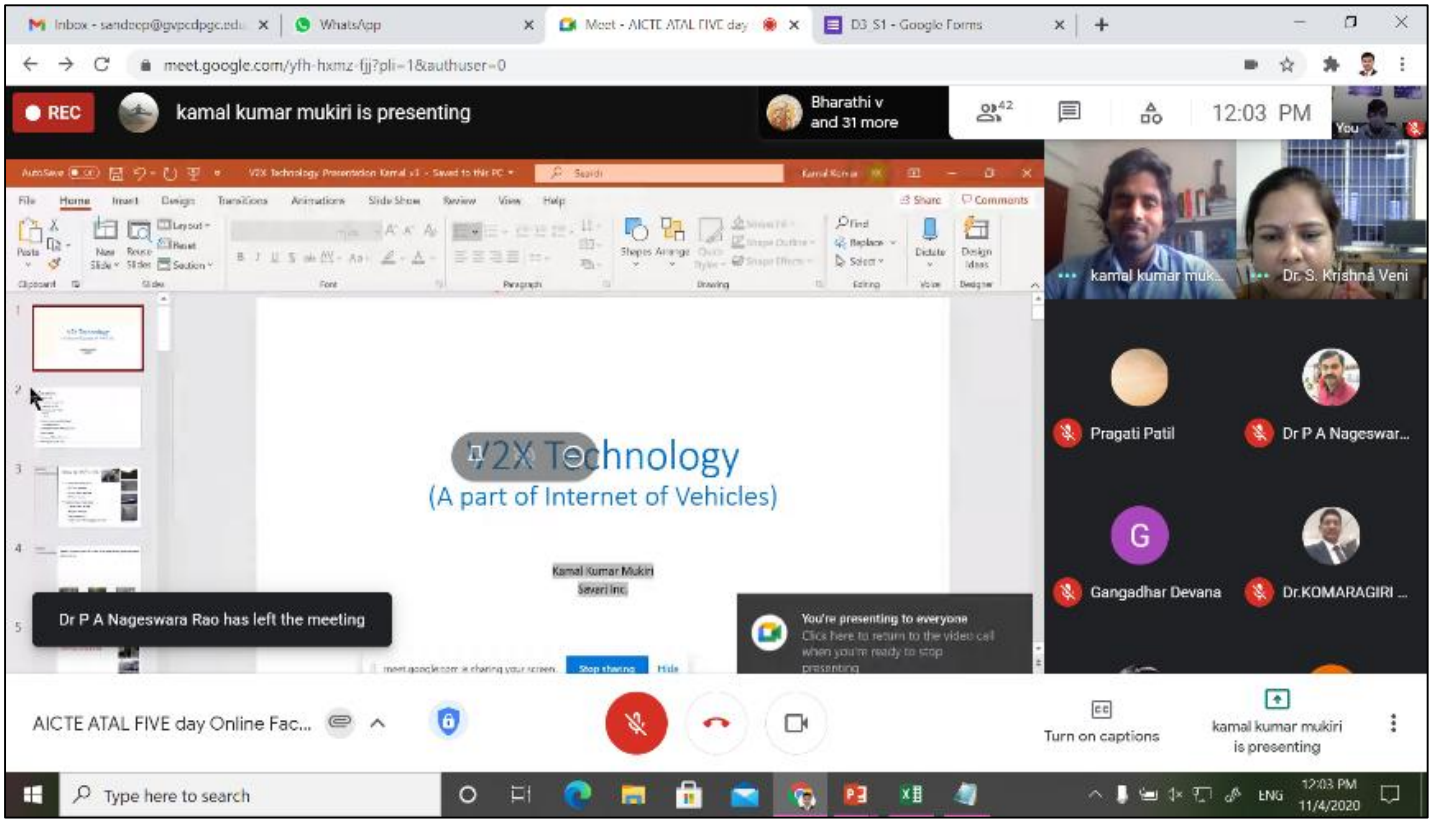

REC
Bapuji Kanaparthi is presenting
sajid shaikh and 42 more
10:14 AM
Internet of Things Story
Number of Steps
Average Speed
Appleton Innovations
You
Bapuji Kanaparthi
Dr. S. Krishna Veni
Mutyala Naidu
Savita Bhosale
Gangadhar Devana
Dr.KOMARAGIRI R...
Dr P A Nageswar...
Type here to search

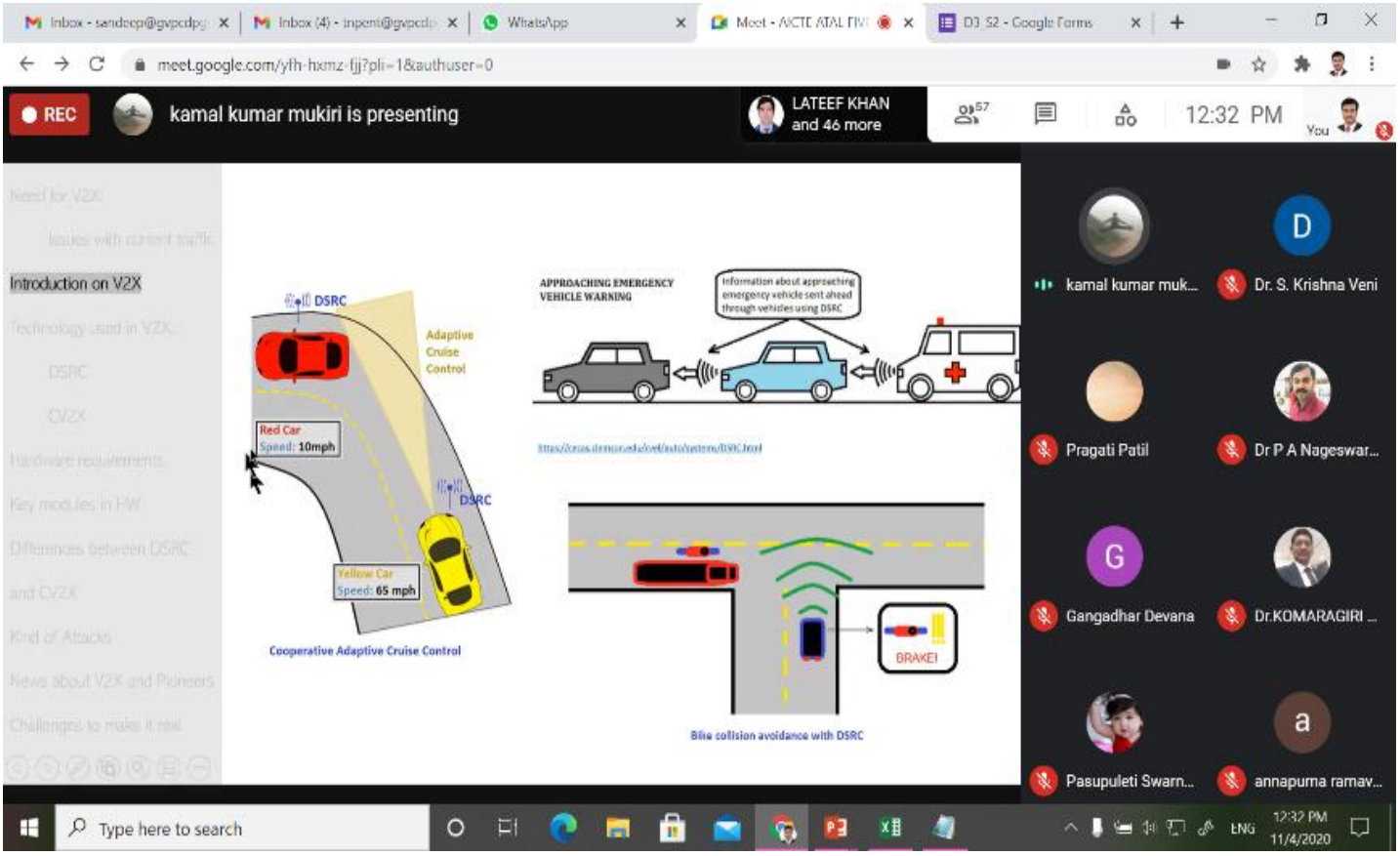

REC
Bapuji Kanaparthi is presenting
Pragati Patil and 50 more
10:41 AM
Node Design
Microcontroller/processor
Sensors/Actuators
Connectivity
Appleton Innovations
You
Bapuji Kanaparthi
Mutyala Naidu
Pragati Patil
Dr P A Nageswara...
Savita Bhosale
Gangadhar Devana
A.Pradeep Kumar
Type here to search

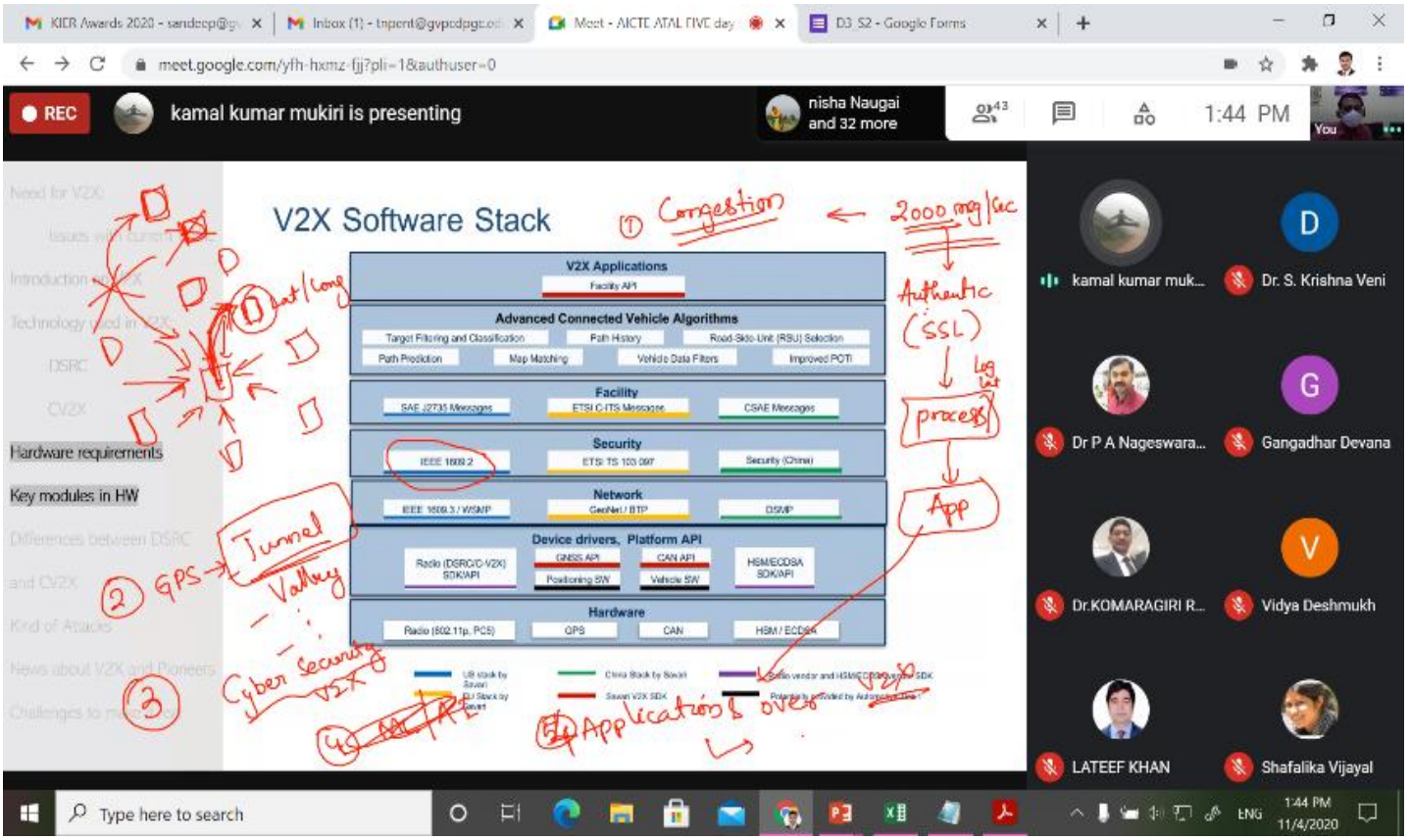

meet.google.com/yfh-hxmz-fjj?pli=1&authuser=0
REC
Bapuji Kanaparthi is presenting
Ravindra Prabhu and 46 more
11:22 AM
You
hello...GVP
^CTraceback (most recent call last):
File "gvp1.py", line 4, in <module>
time.sleep(1)
KeyboardInterrupt
pi@raspberrypi:~ $ nano gvp1.py
pi@raspberrypi:~ $ python gvp1.py
Bapuji Kanaparthi
Mutyala Naidu
Pragati Patil
Gangadhar Devana
Dr P A Nageswara...
Dr. S. Krishna Veni
Suman Prakash
narendra kumar
Activate Windows
Type here to search
ENG
11:22 AM
11/4/2020

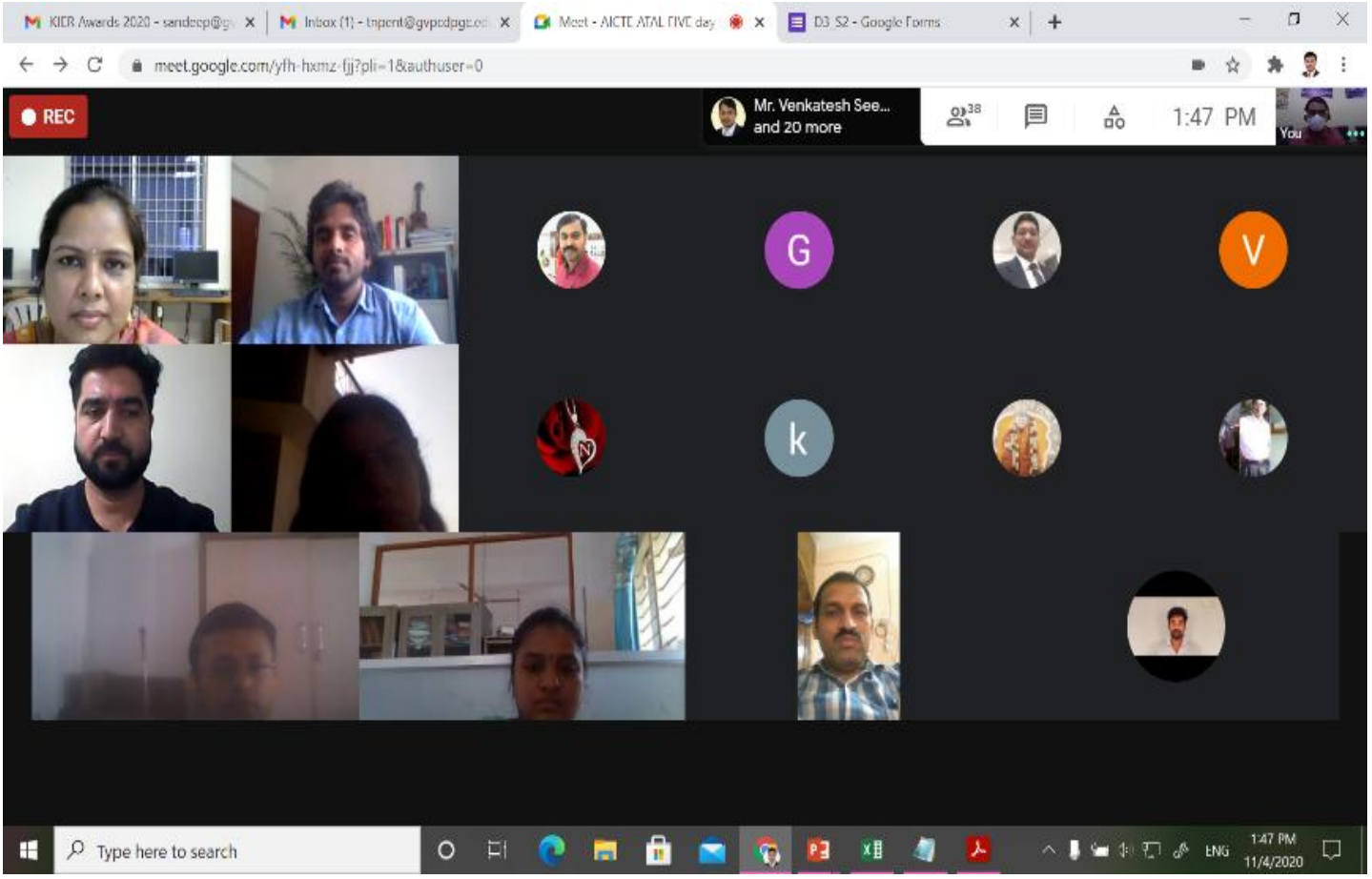

meet.google.com/yfh-hxmz-fjj?pli=1&authuser=0
REC
chakradharsudhir ama... and 14 more
11:45 AM
You
Type here to search
ENG
11:45 AM
11/4/2020

Day 3 Session 2

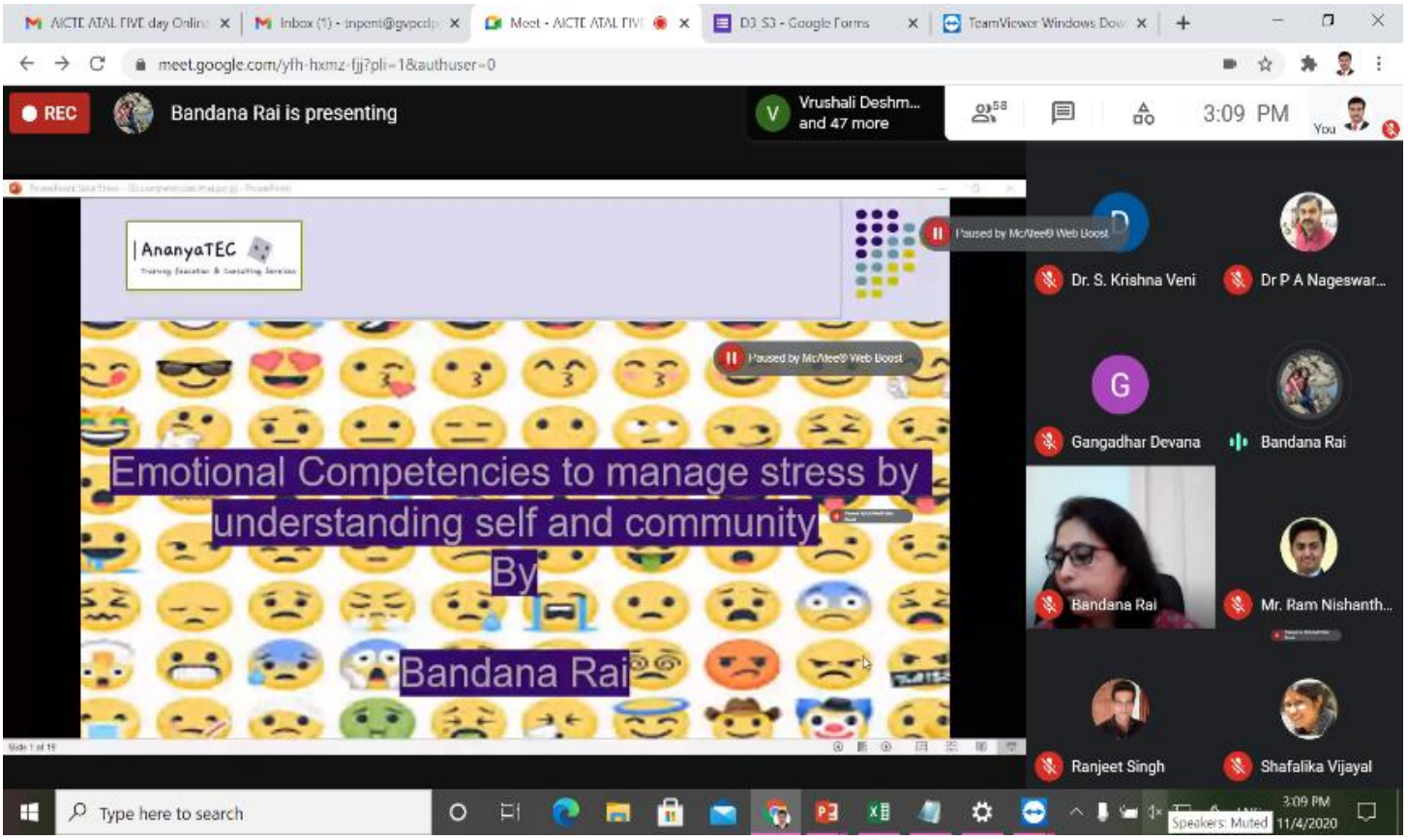


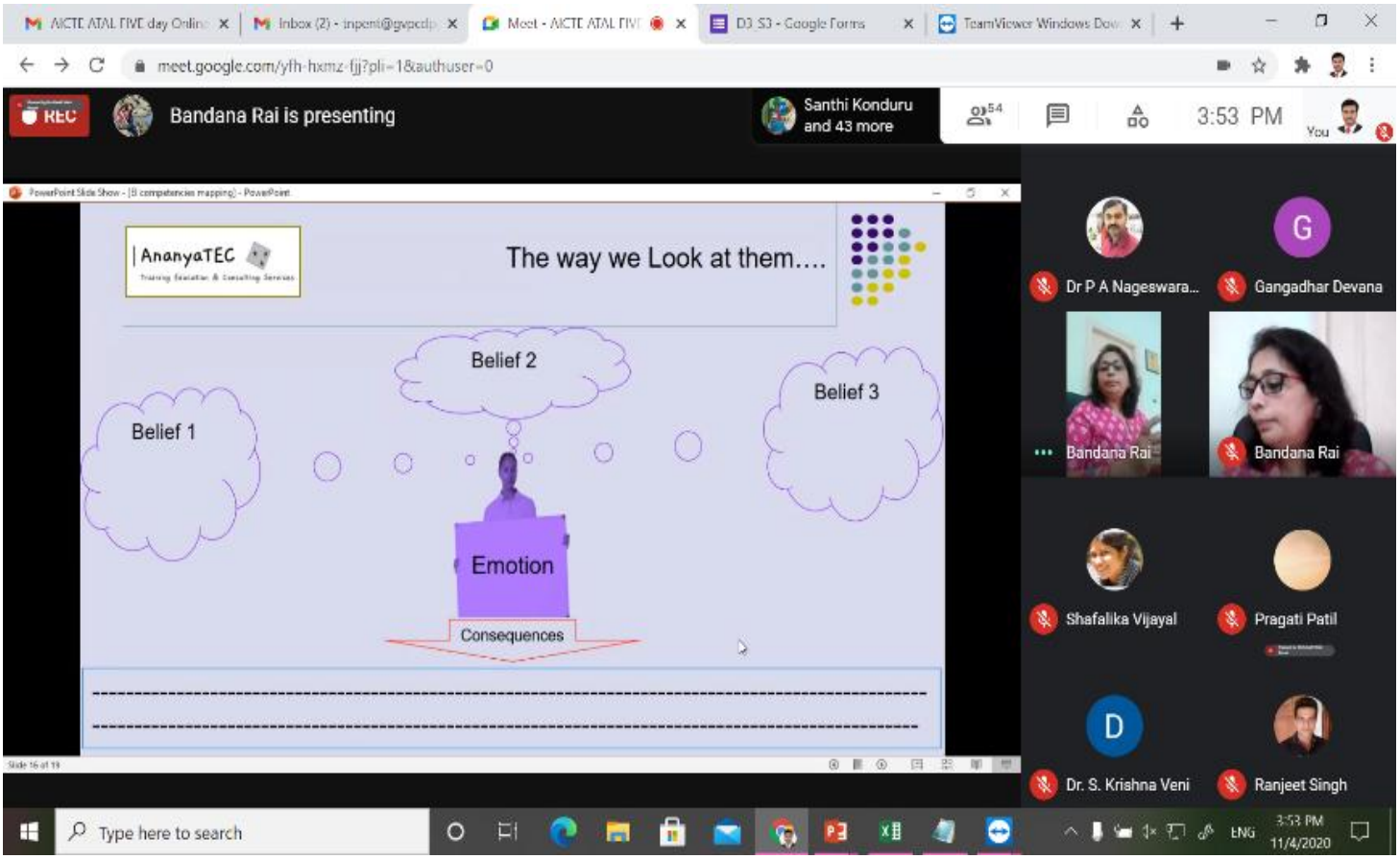


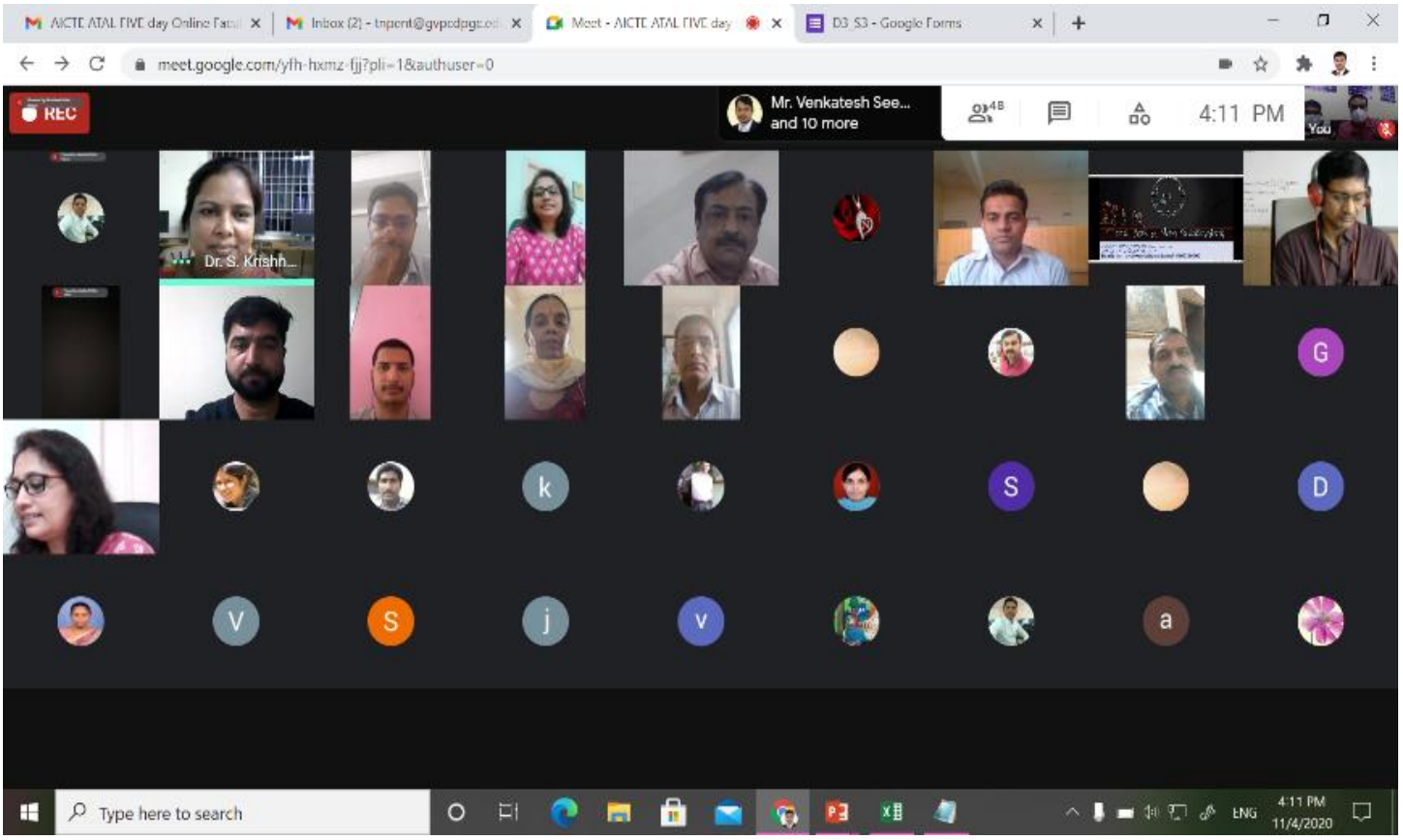

REC
kamal kumar mukiri is presenting
nisha Naugai and 32 more
1:44 PM
V2X Software Stack
V2X Applications
Advanced Connected Vehicle Algorithms
Facility
Security
Network
Device drivers, Platform API
Hardware
Congestion
2000 msg/sec
Authentic (SSL)
process
App
Tunnel
Valley
GPS
Cyber security V2X
Applications overs
kamal kumar muk...
Dr. S. Krishna Veni
Dr P A Nageswara...
Gangadhar Devana
Dr.KOMARAGIRI R...
Vidya Deshmukh
LATEEF KHAN
Shafalika Vijayal
Type here to search
1:44 PM
11/4/2020


REC
Mr. Venkatesh See... and 20 more
1:47 PM
Type here to search
1:47 PM
11/4/2020

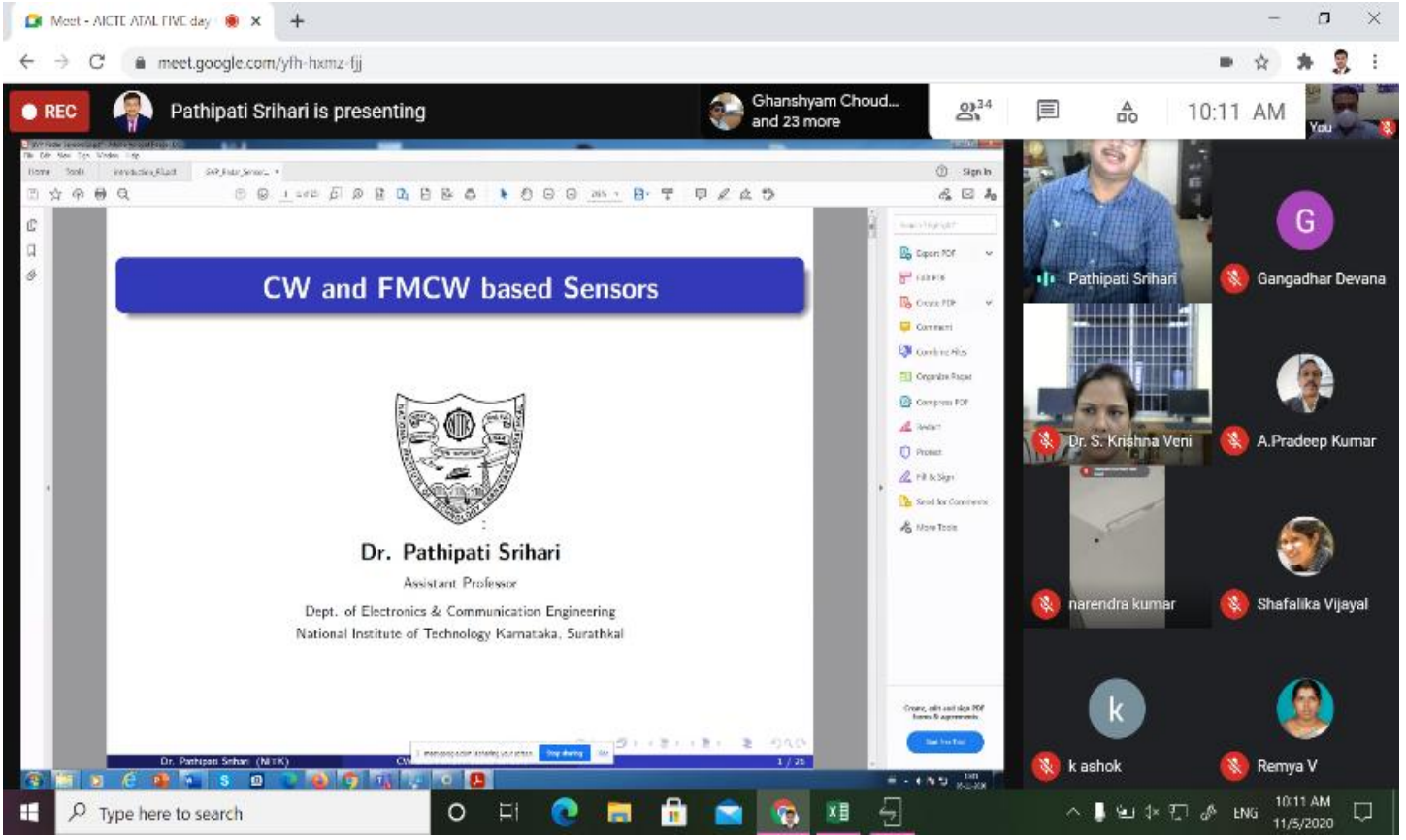
Day 3 Session 3

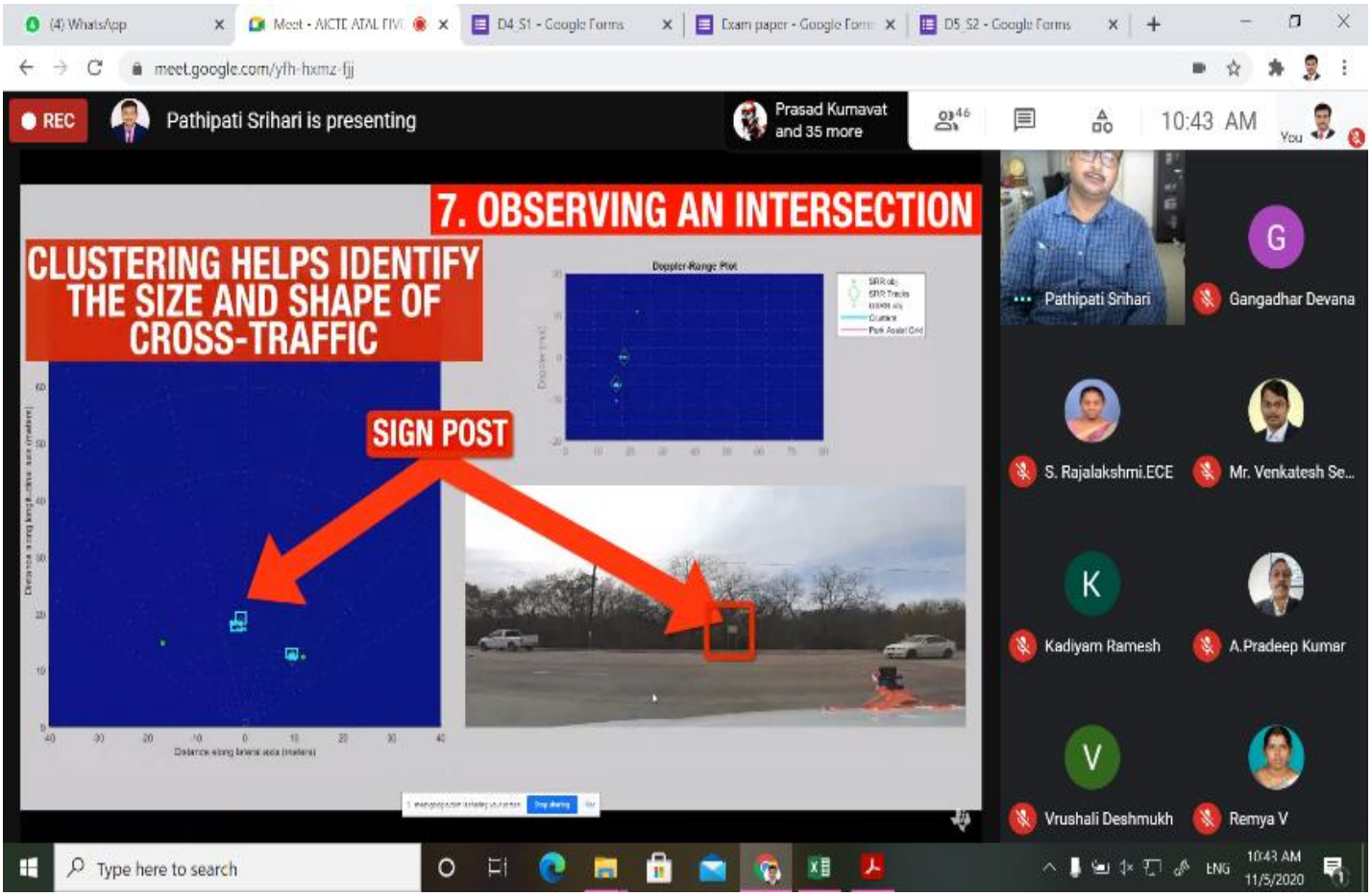


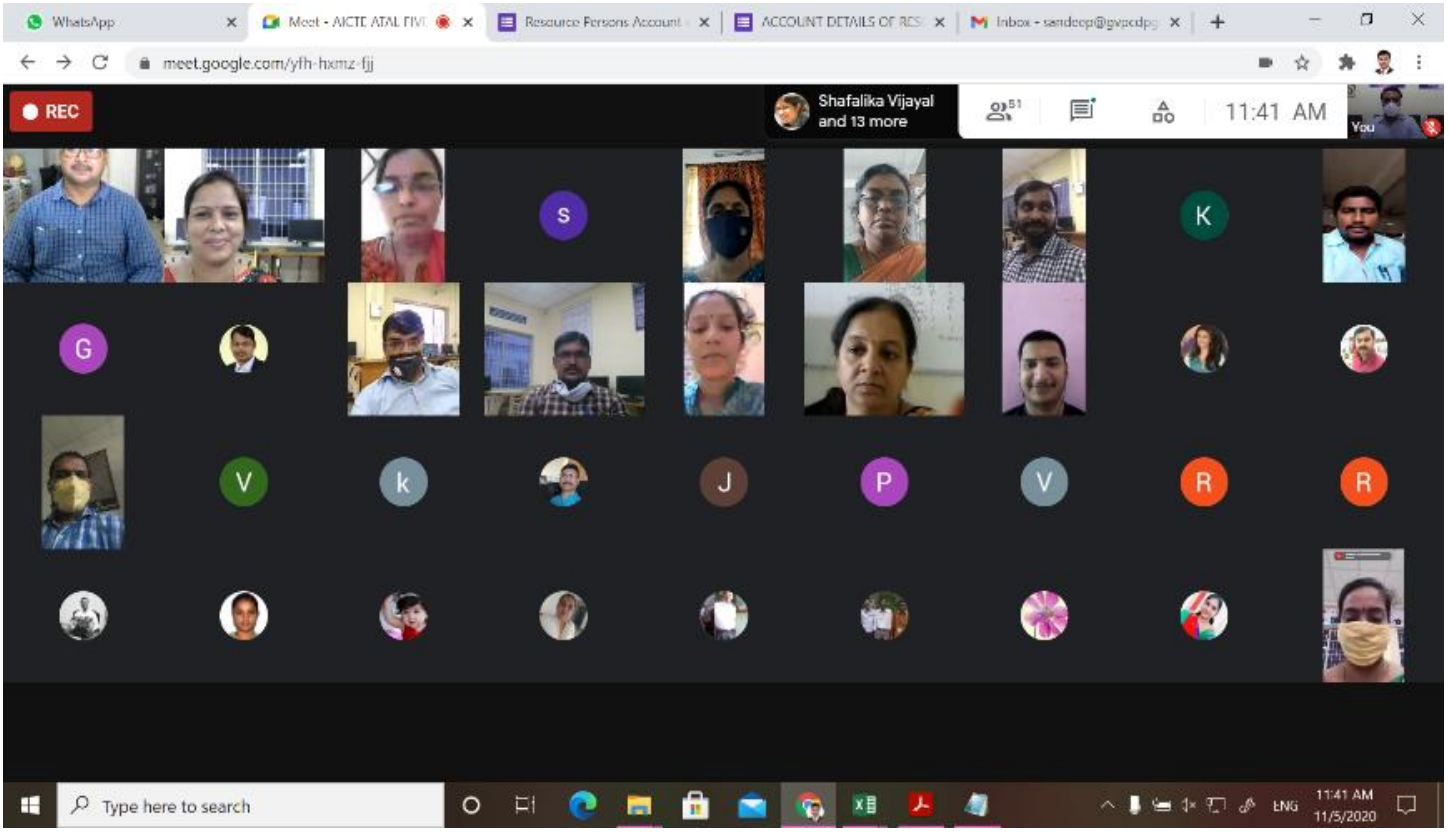




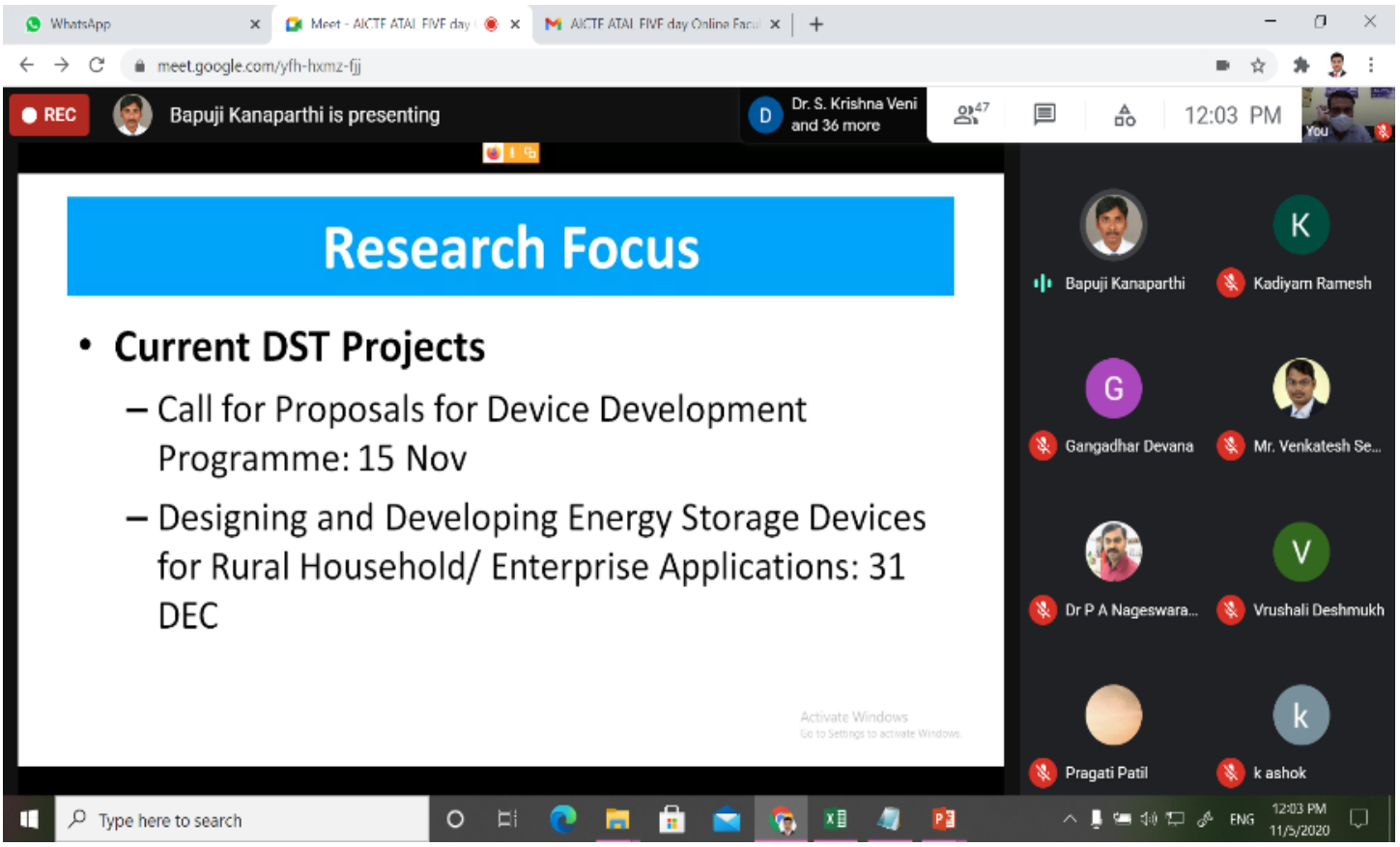
Day 4 Session 1

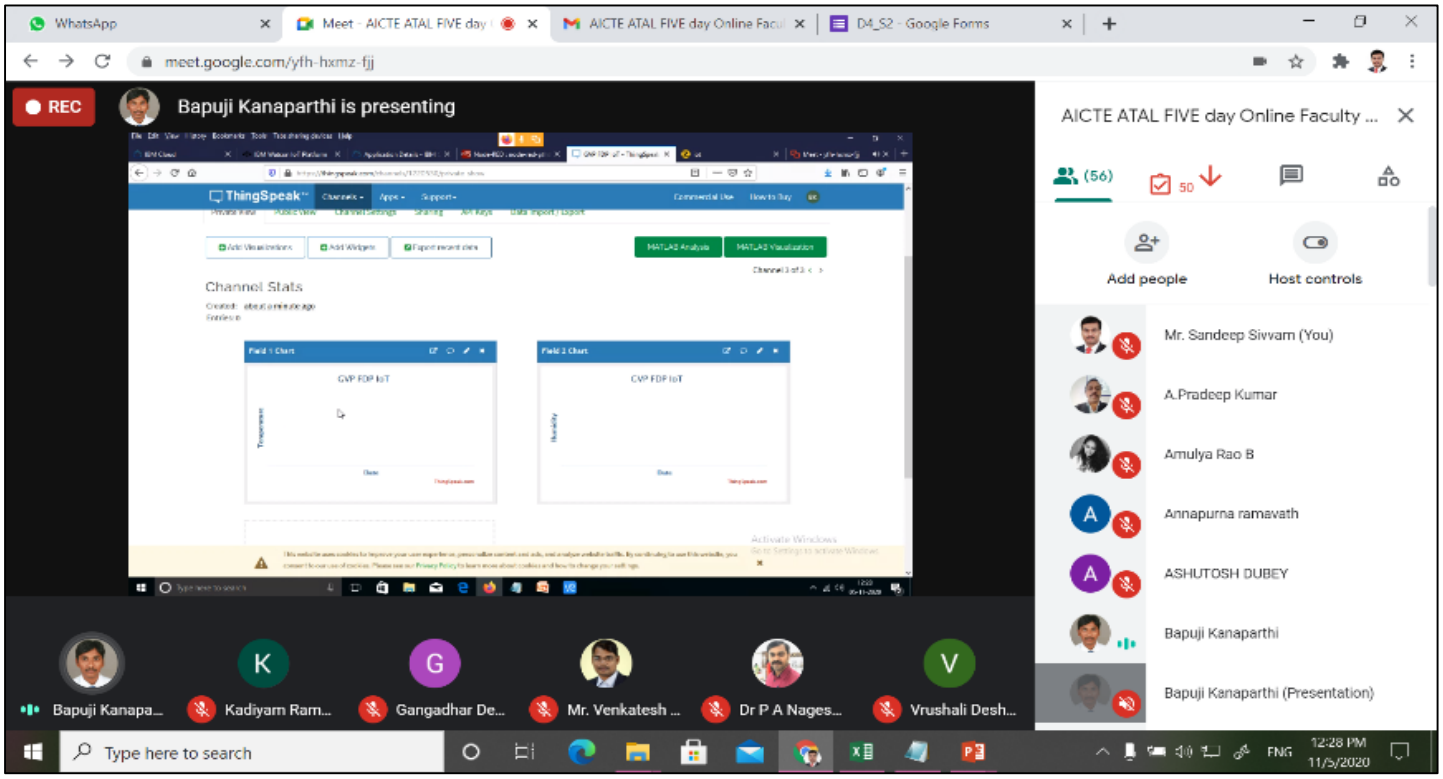


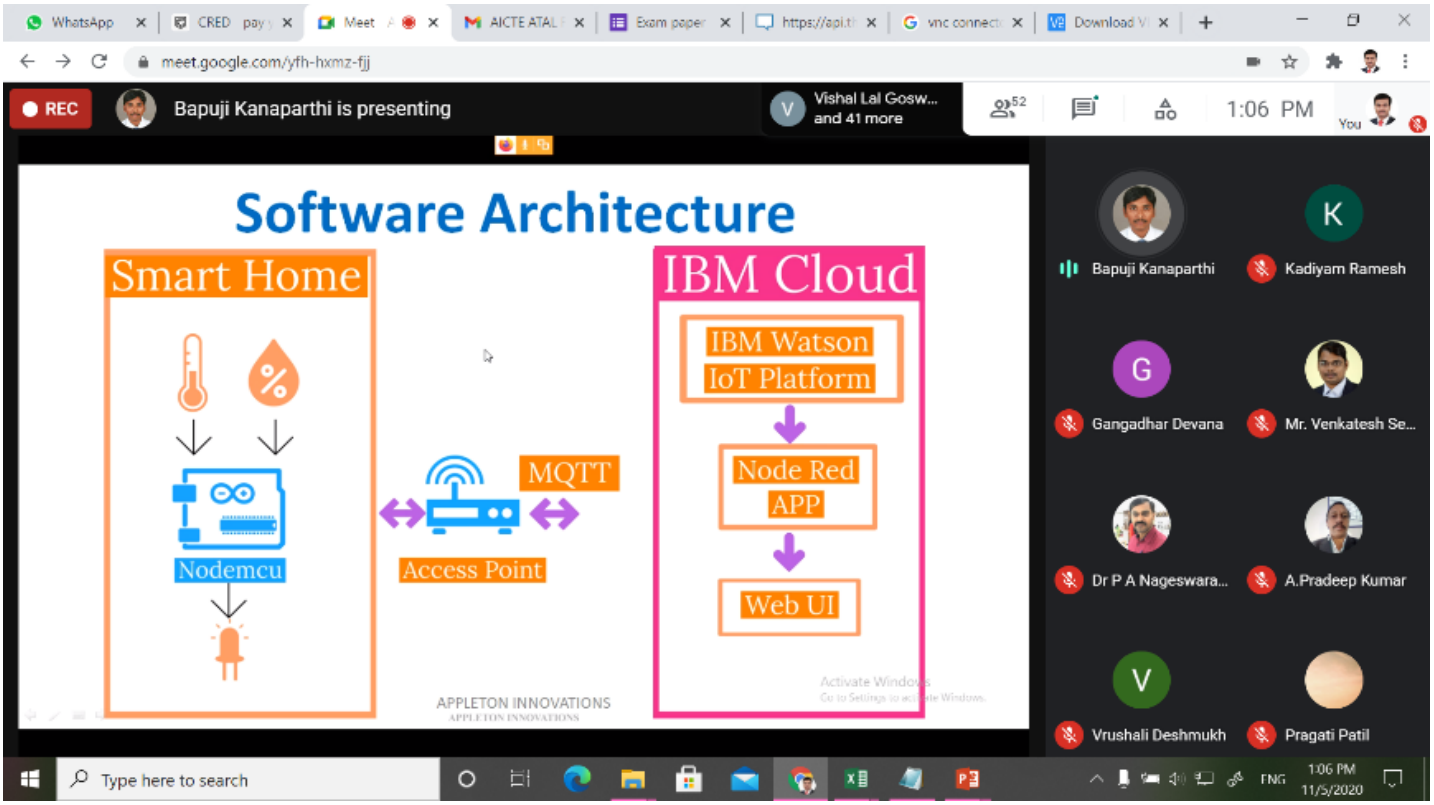

REC
Pathipati Srihari is presenting
Prasad Kumavat and 35 more
10:43 AM
7. OBSERVING AN INTERSECTION
CLUSTERING HELPS IDENTIFY THE SIZE AND SHAPE OF CROSS-TRAFFIC
SIGN POST
Pathipati Srihari
Gangadhar Devana
S. Rajalakshmi.ECE
Mr. Venkatesh Se...
Kadiyam Ramesh
A.Pradeep Kumar
Vrushali Deshmukh
Remya V
Type here to search

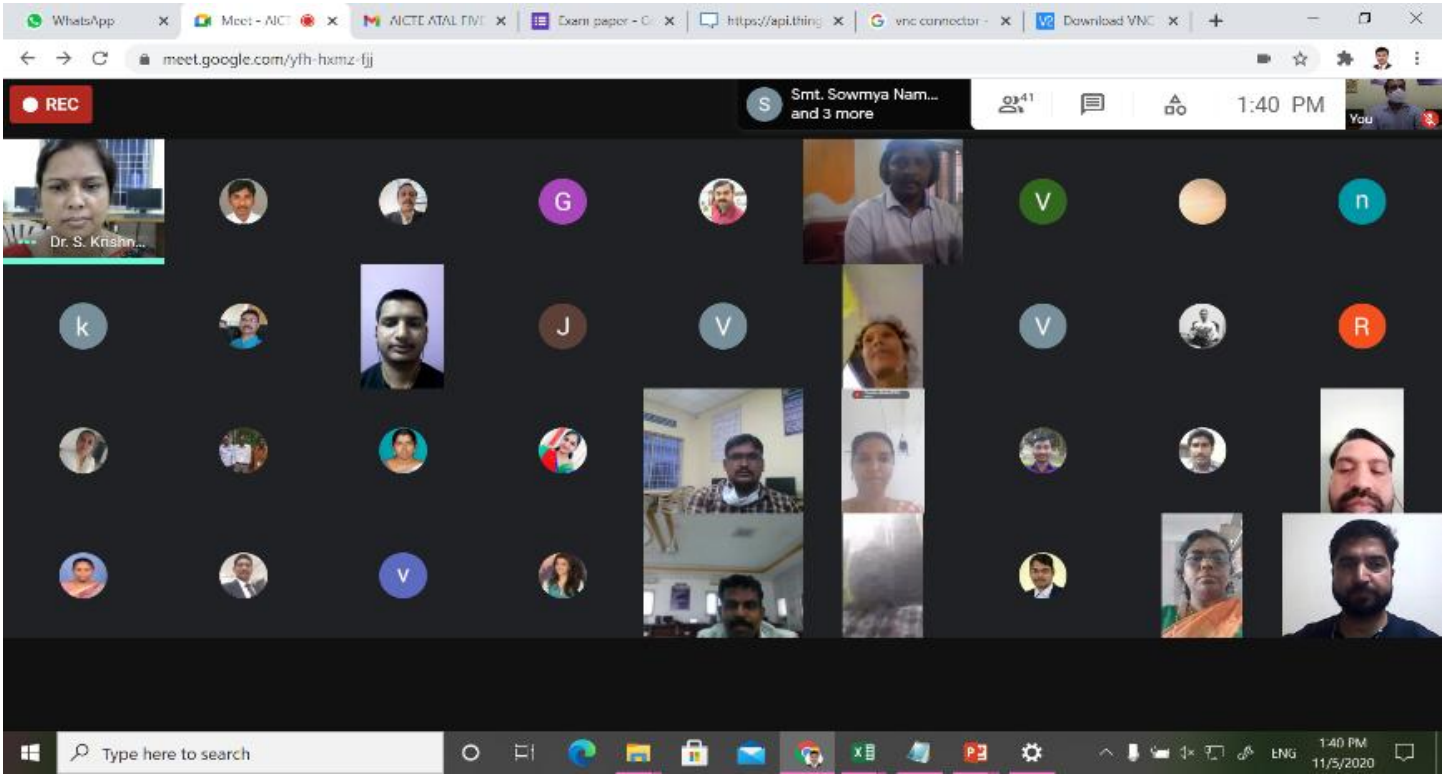

REC
Shafalika Vijayal and 13 more
11:41 AM
Type here to search

Day 4 Session 2

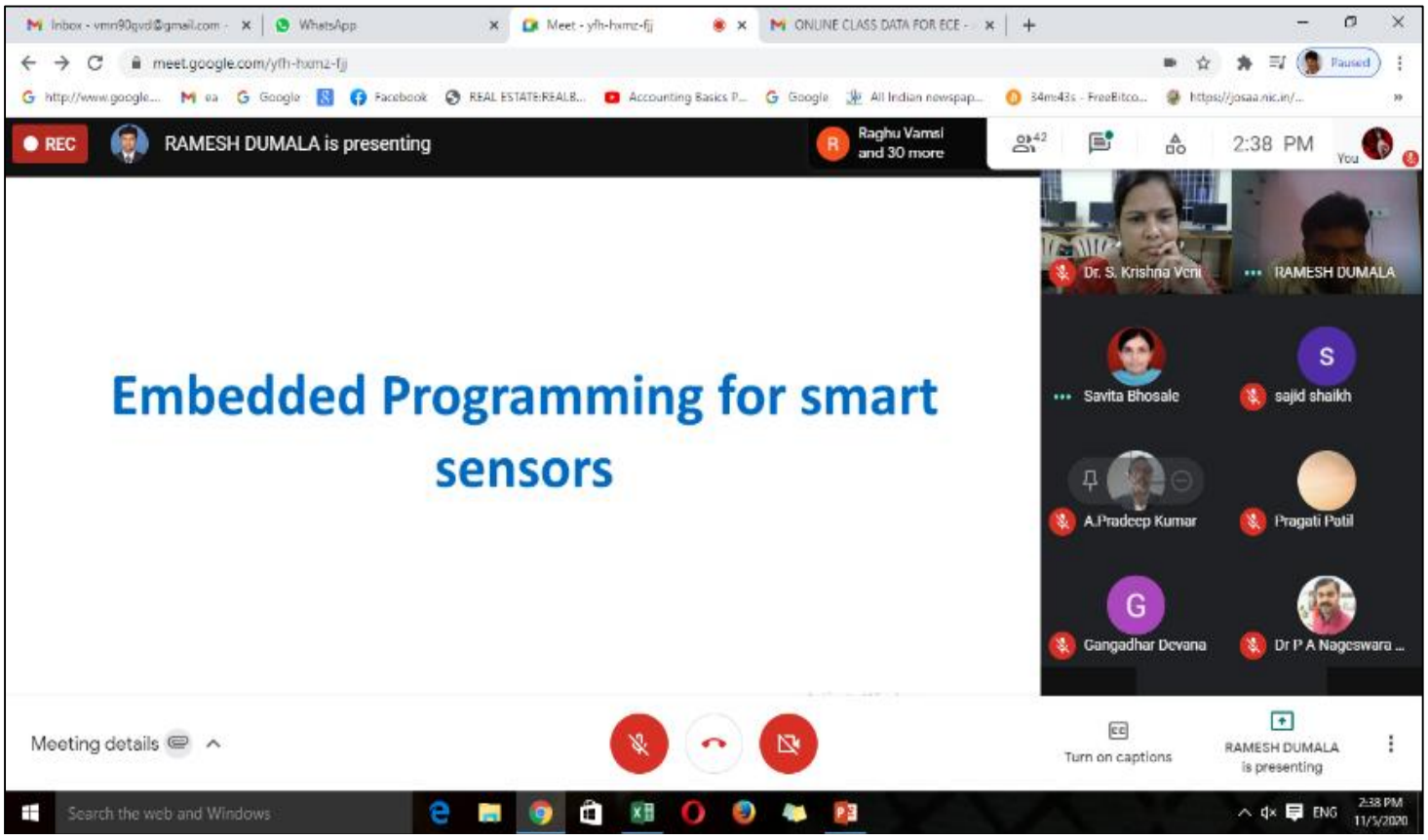


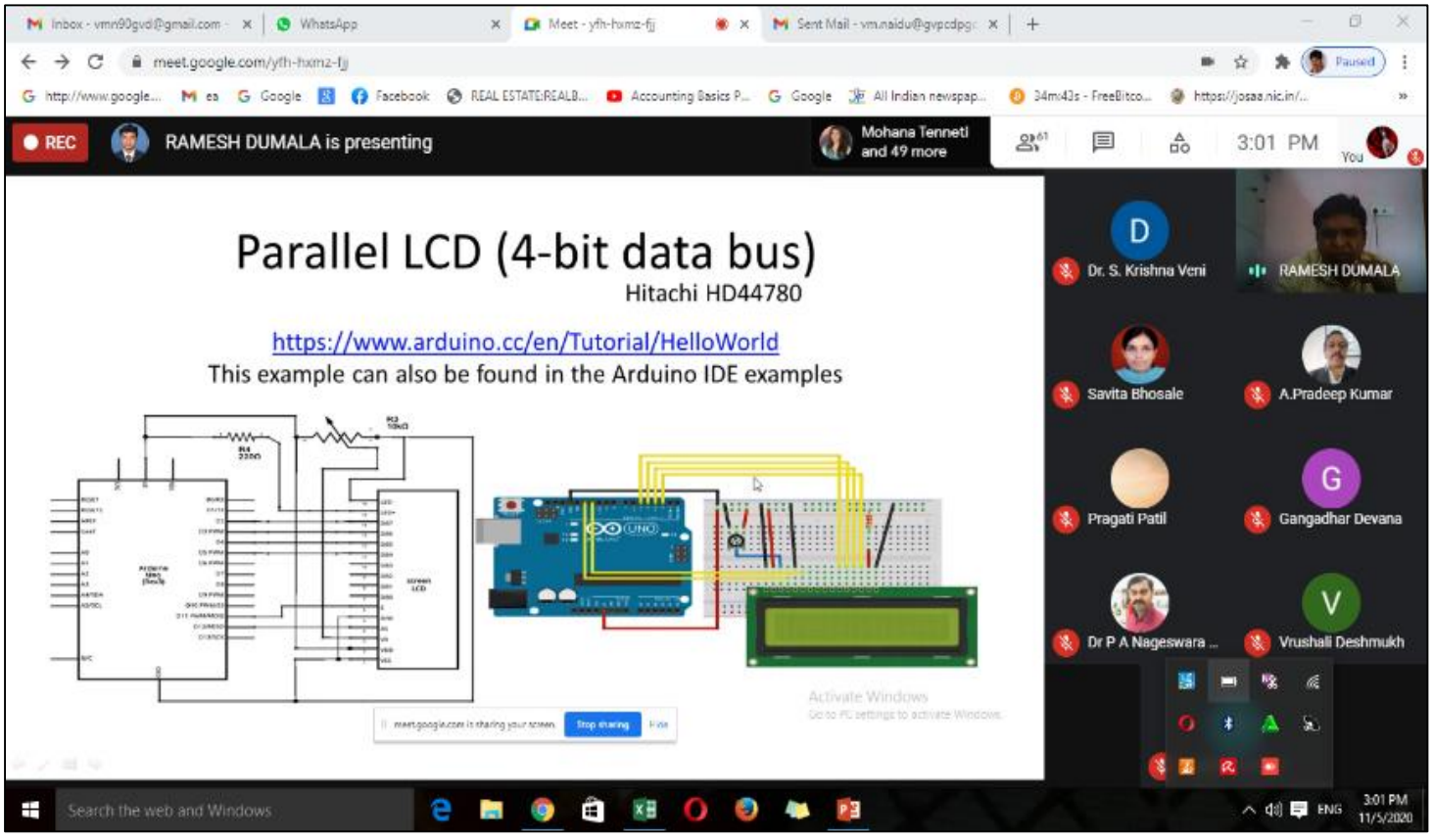


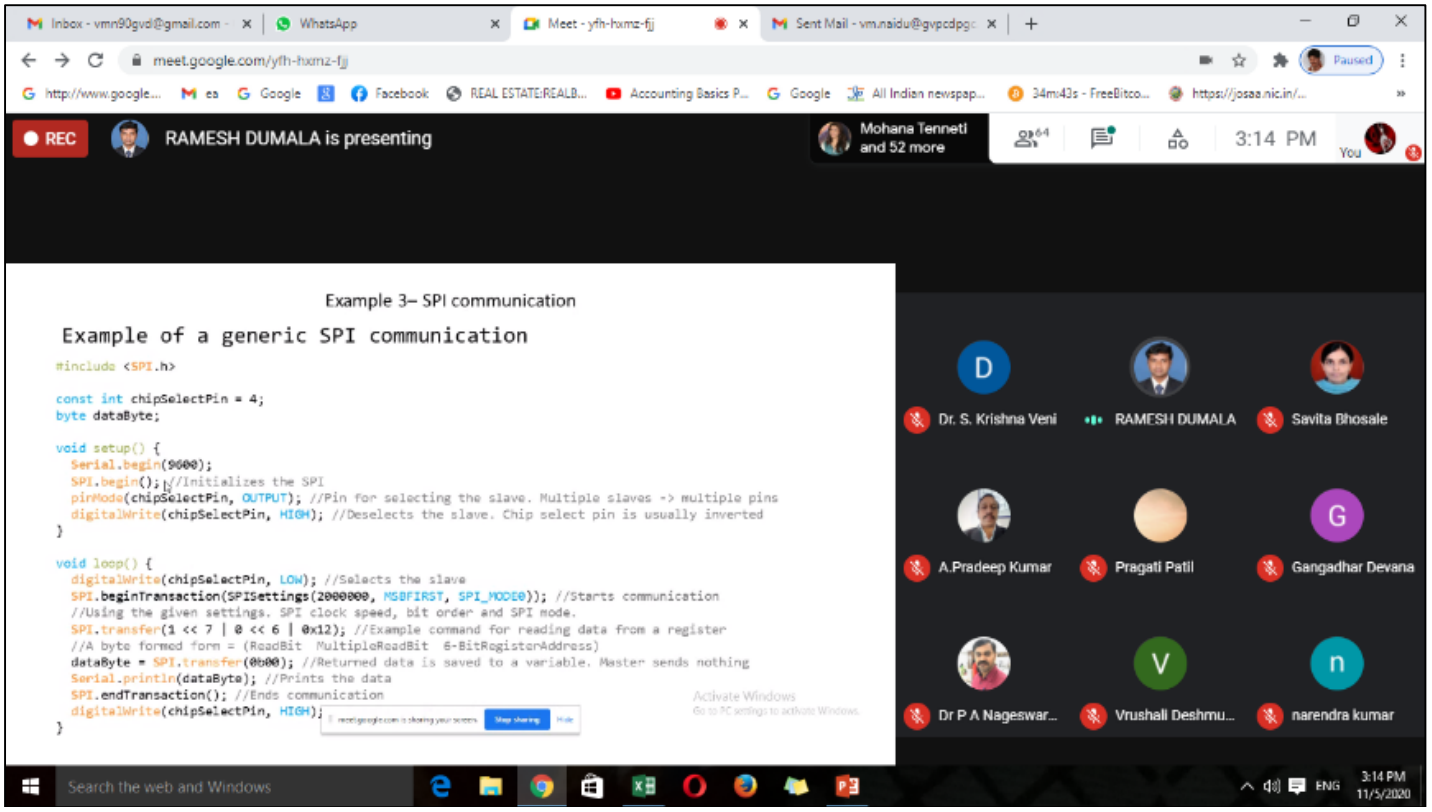

meet.google.com/yfh-hxmz-fjj
REC
Bapuji Kanaparthi is presenting
Vishal Lal Gosw... and 41 more
1:06 PM
Software Architecture
Smart Home
Nodemcu
MQTT
Access Point
IBM Cloud
IBM Watson IoT Platform
Node Red APP
Web UI
APPLETON INNOVATIONS
Bapuji Kanaparthi
Kadiyam Ramesh
Gangadhar Devana
Mr. Venkatesh Se...
Dr P A Nageswara...
A.Pradeep Kumar
Vrushali Deshmukh
Pragati Patil
Type here to search
1:06 PM
11/5/2020


meet.google.com/yfh-hxmz-fjj
REC
Smt. Sowmya Nam... and 3 more
1:40 PM
Dr. S. Krishn...
Type here to search
1:40 PM
11/5/2020

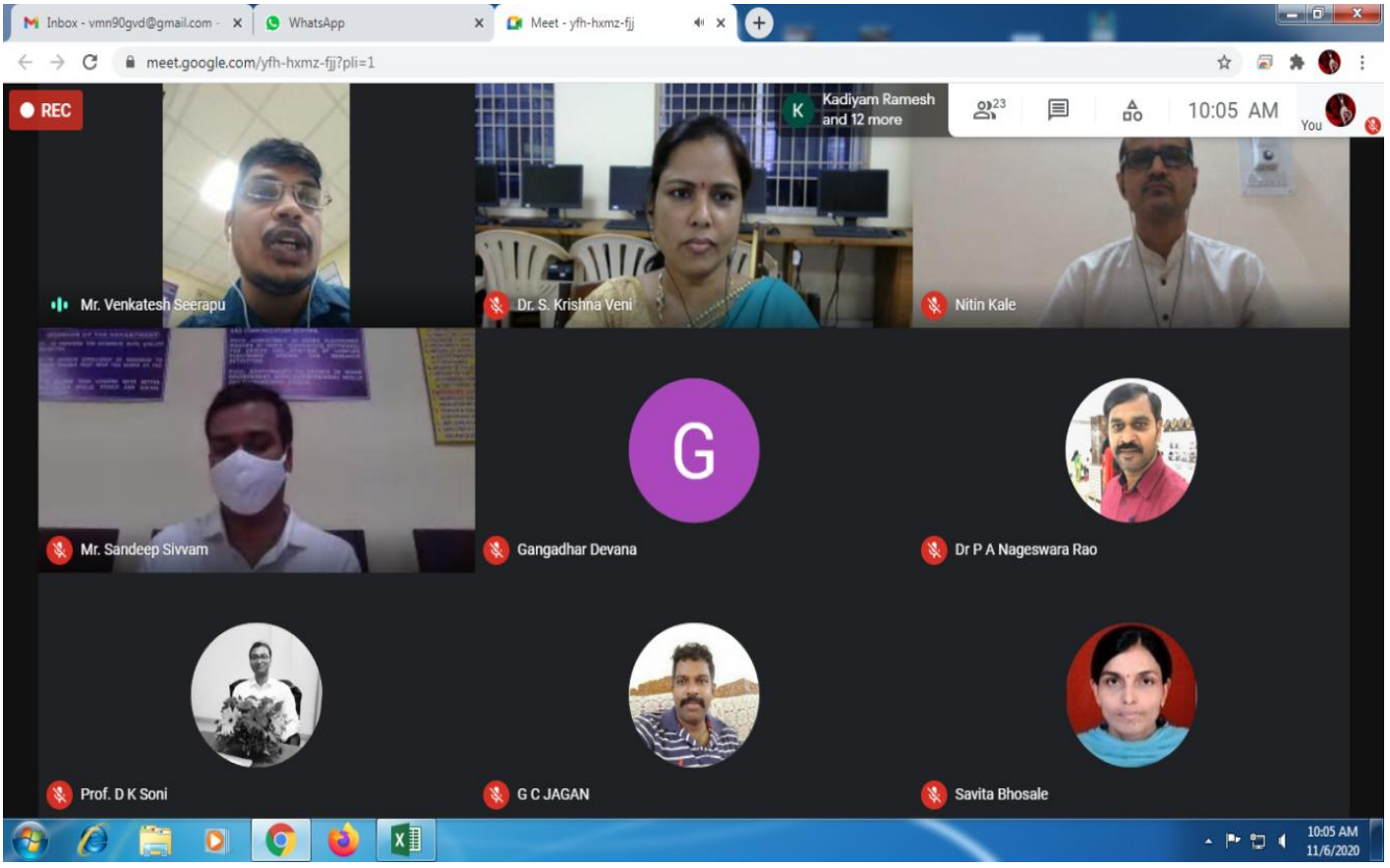
Day 4 Session 3

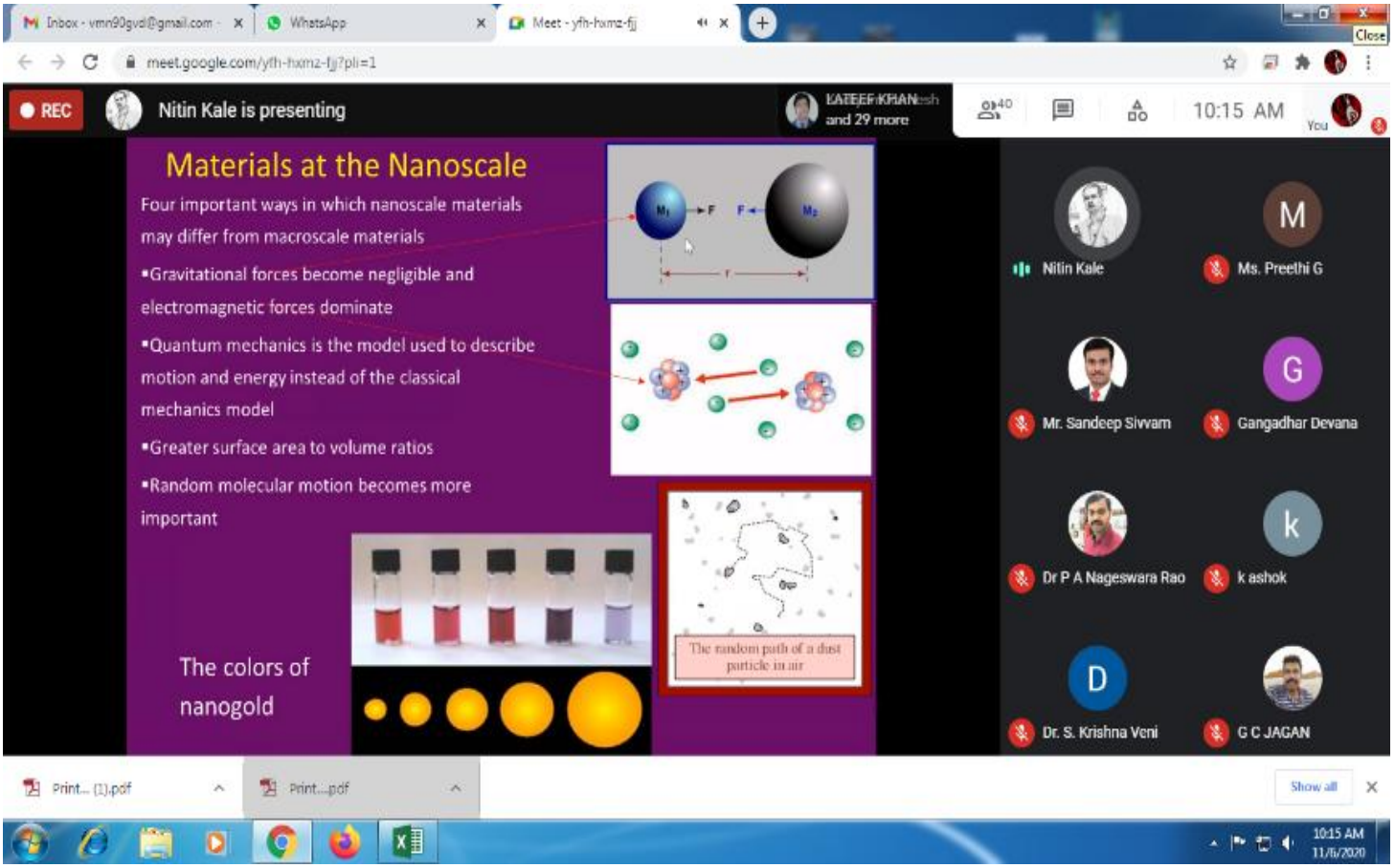


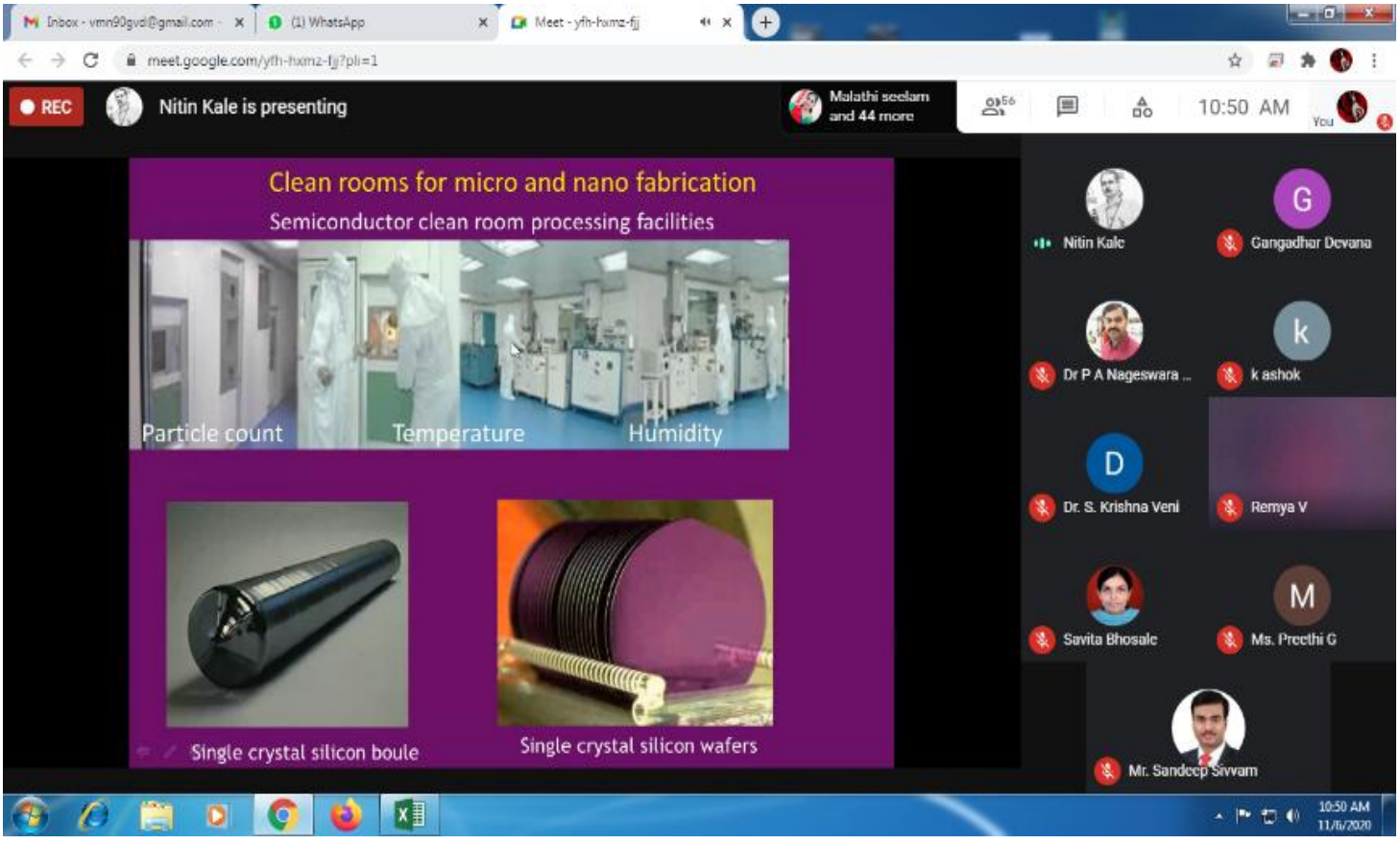




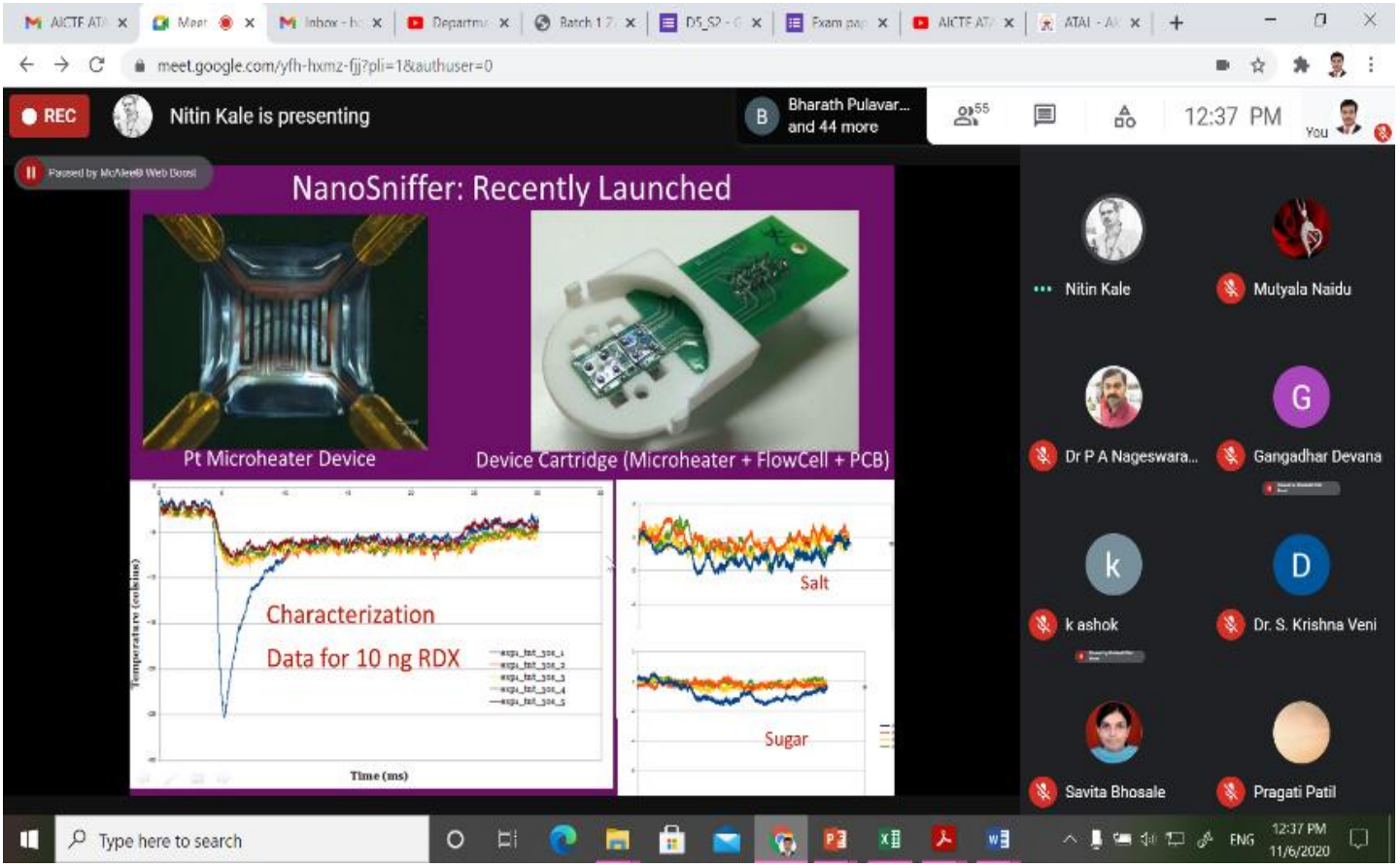
Day 5 Session 1

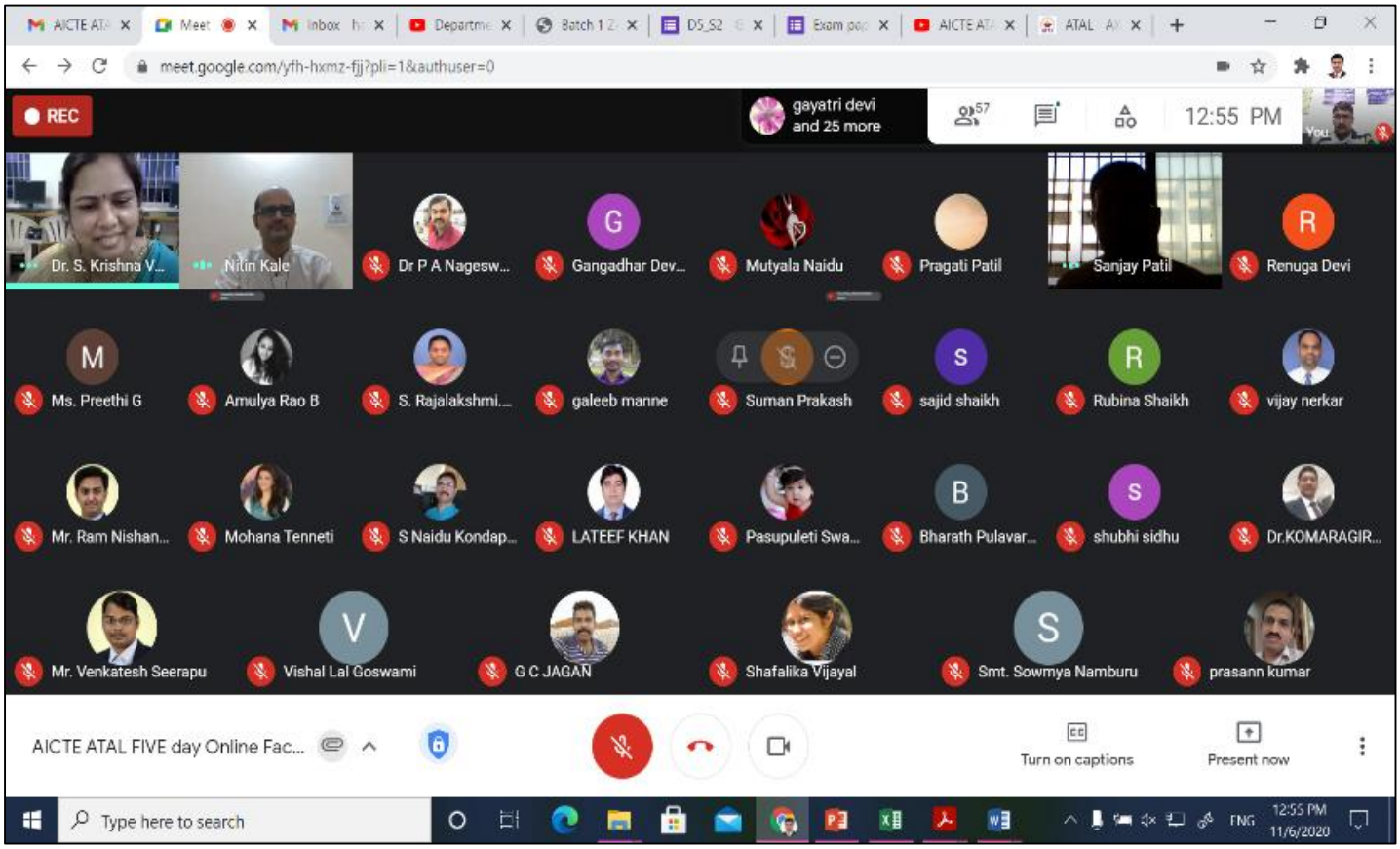



REC
Nitin Kale is presenting
and 29 more
10:15 AM
Materials at the Nanoscale
Four important ways in which nanoscale materials may differ from macroscale materials
▪Gravitational forces become negligible and electromagnetic forces dominate
▪Quantum mechanics is the model used to describe motion and energy instead of the classical mechanics model
▪Greater surface area to volume ratios
▪Random molecular motion becomes more important
The colors of nanogold
The random path of a dust particle in air
Nitin Kale
Ms. Preethi G
Mr. Sandeep Sivvam
Gangadhar Devana
Dr P A Nageswara Rao
k ashok
Dr. S. Krishna Veni
G C JAGAN

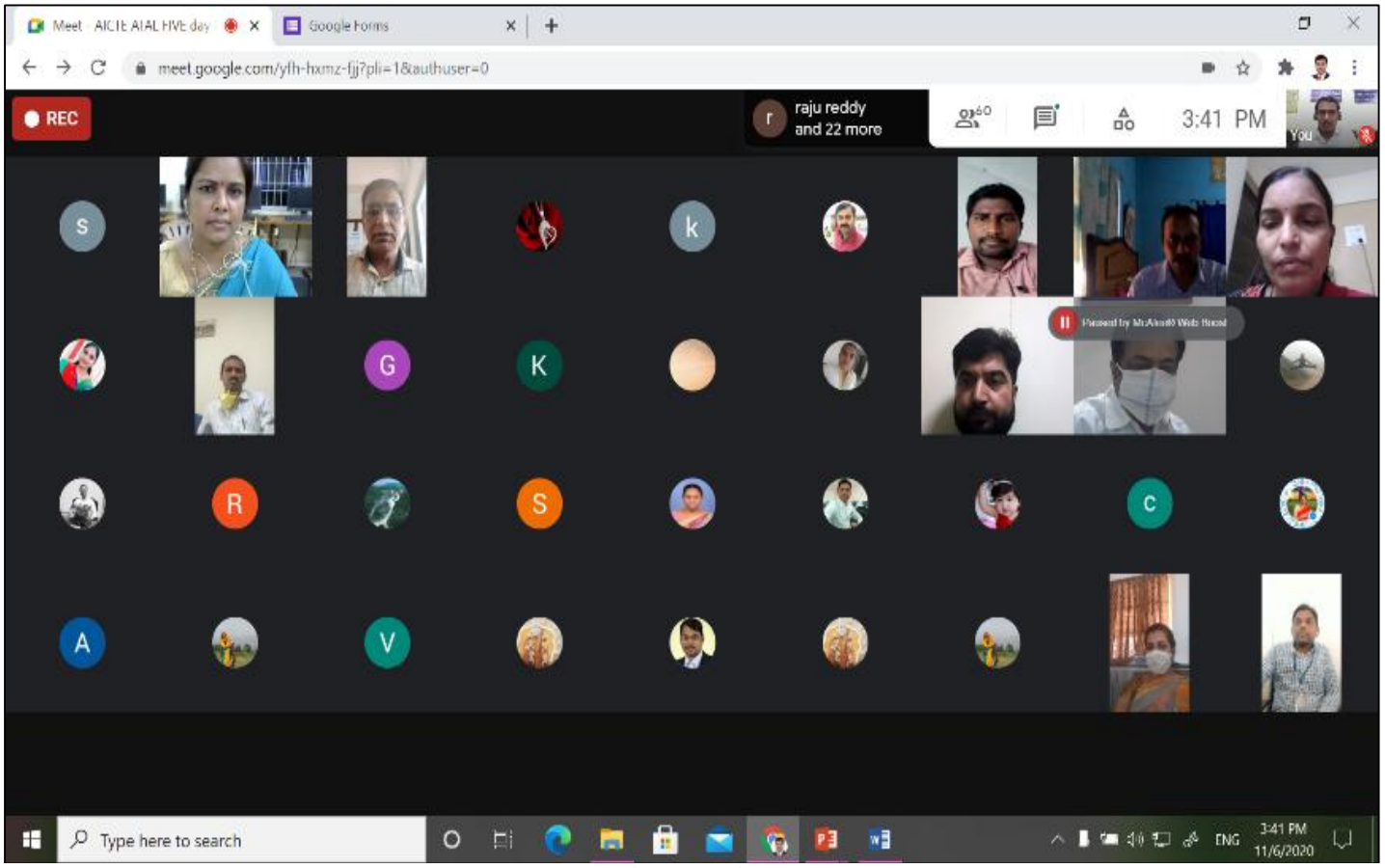

REC
Nitin Kale is presenting
and 44 more
10:50 AM
Clean rooms for micro and nano fabrication
Semiconductor clean room processing facilities
Particle count
Temperature
Humidity
Single crystal silicon boule
Single crystal silicon wafers
Nitin Kale
Gangadhar Devana
Dr P A Nageswara ...
k ashok
Dr. S. Krishna Veni
Remya V
Savita Bhosale
Ms. Preethi G
Mr. Sandeep Sivvam

Day 5 Session 2

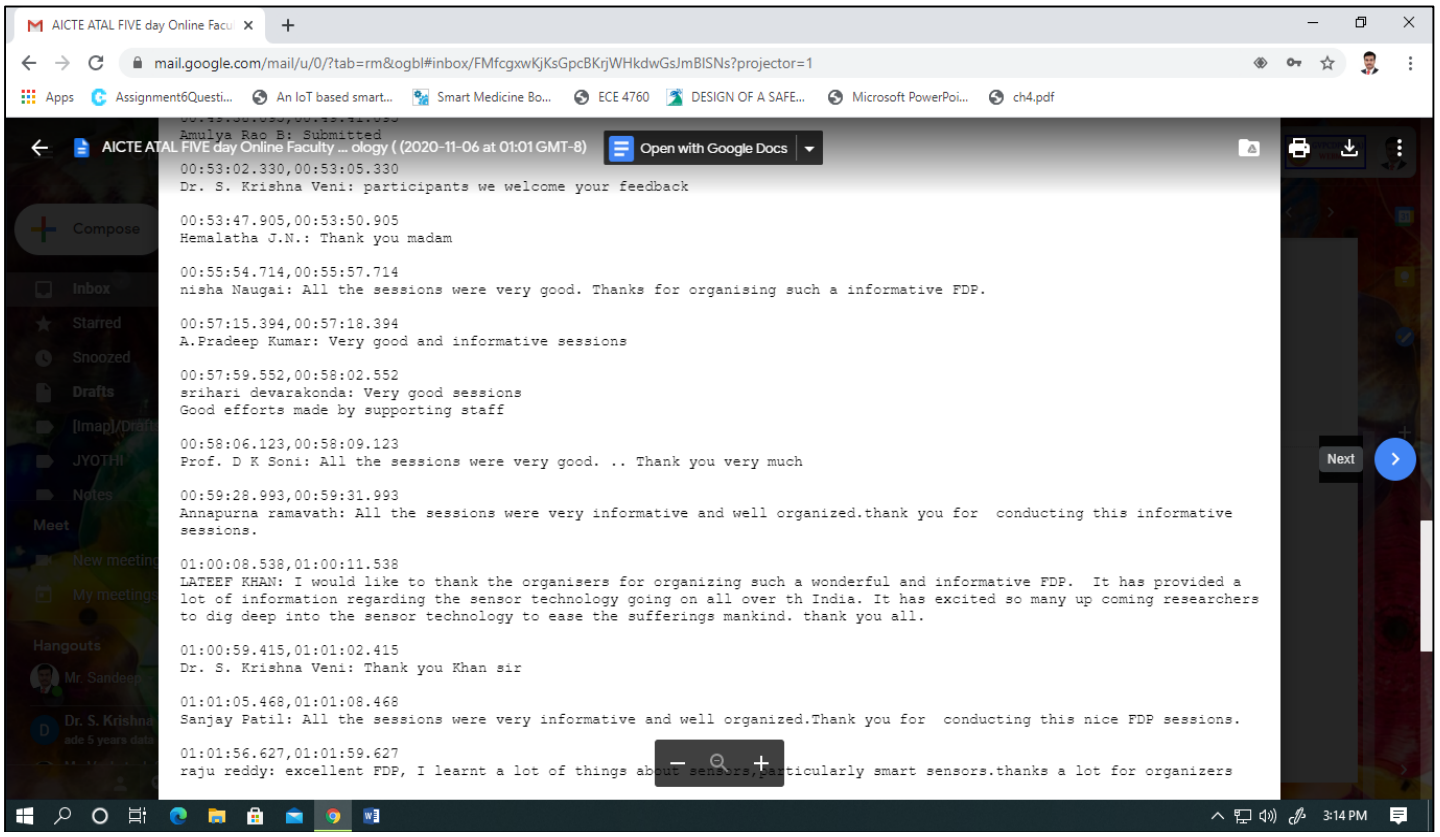


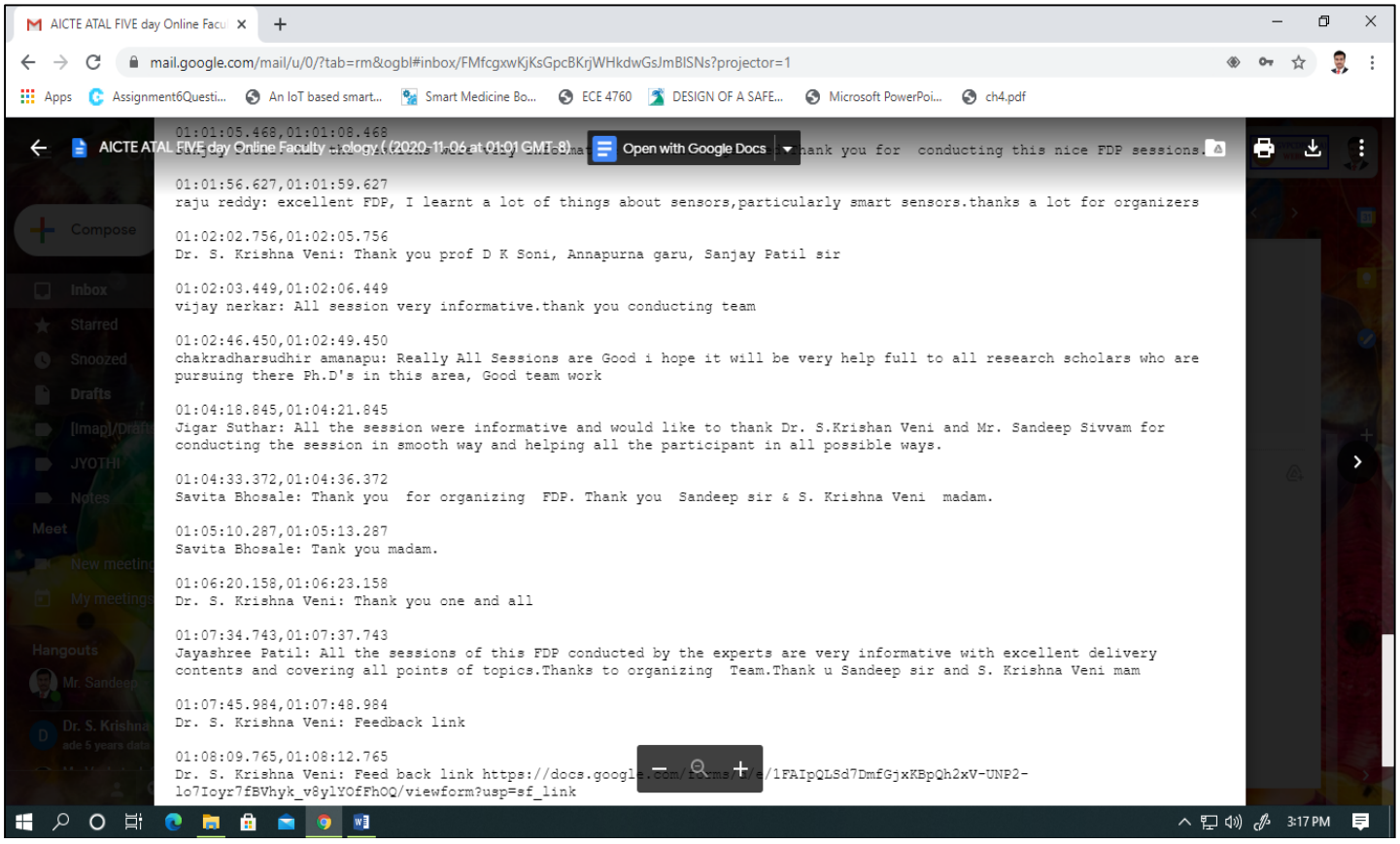


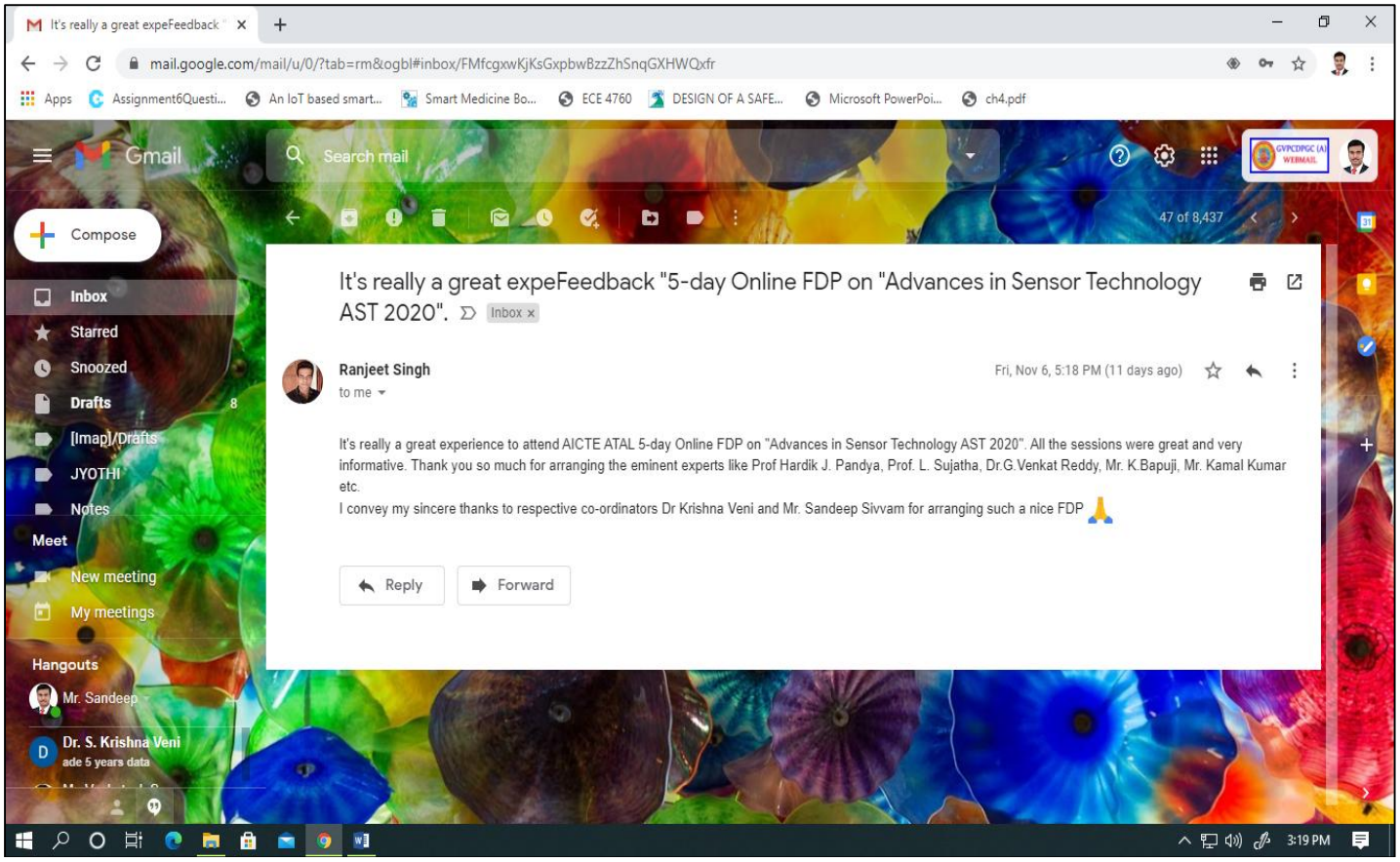
Day 5 Session 3



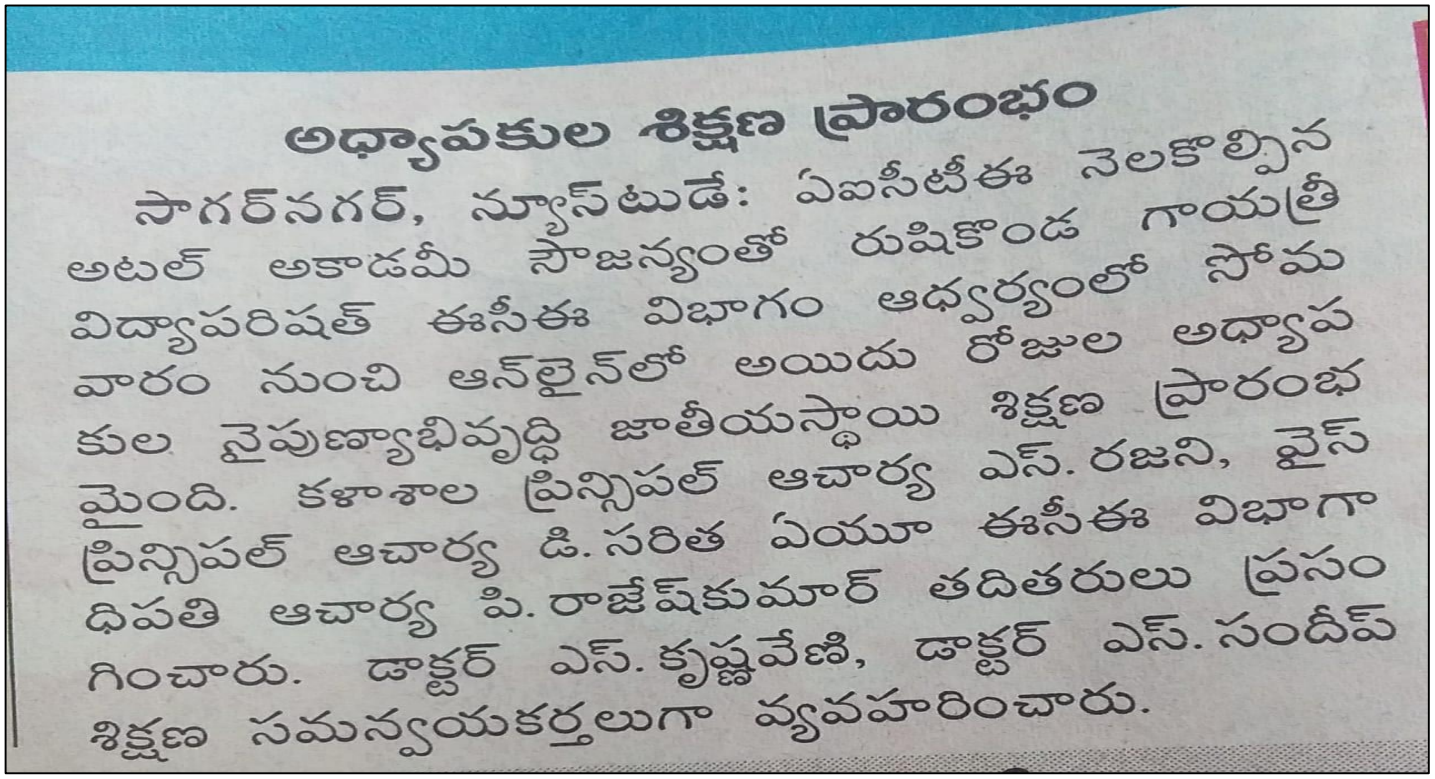
Participants Feedback







Press Clippings

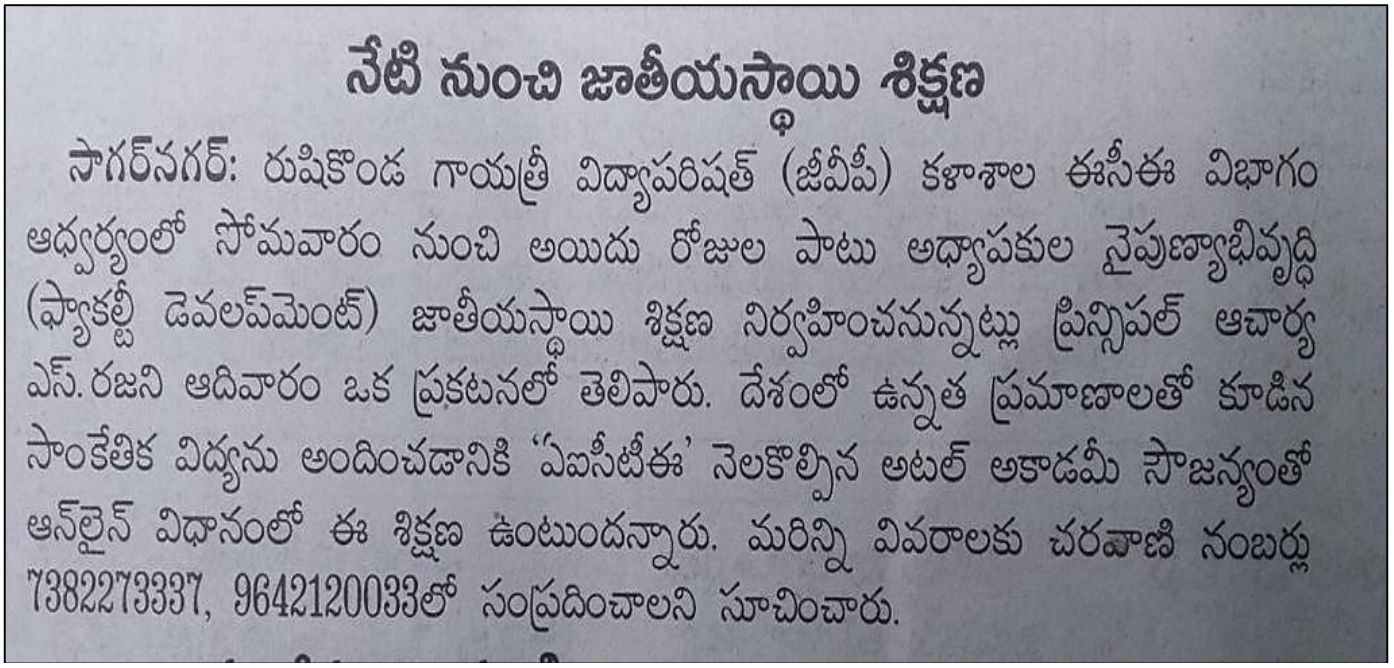


అధ్యాపకుల శిక్షణ ప్రారంభం

సాగర్‌నగర్, న్యూస్‌టుడే: ఏఐసీటీఈ నెలకొల్పిన అటల్ అకాడమీ సౌజన్యంతో రుషికొండ గాయత్రీ విద్యాపరిషత్ ఈసీఈ విభాగం ఆధ్వర్యంలో సోమవారం నుంచి ఆన్‌లైన్‌లో అయిదు రోజుల అధ్యాపకుల నైపుణ్యాభివృద్ధి జాతీయస్థాయి శిక్షణ ప్రారంభమైంది. కళాశాల ప్రిన్సిపల్ ఆచార్య ఎస్. రజని, వైస్ ప్రిన్సిపల్ ఆచార్య డి. సరిత ఏయూ ఈసీఈ విభాగాధిపతి ఆచార్య పి. రాజేష్‌కుమార్ తదితరులు ప్రసంగించారు. డాక్టర్ ఎస్. కృష్ణవేణి, డాక్టర్ ఎస్. సందీప్ శిక్షణ సమన్వయకర్తలుగా వ్యవహరించారు.

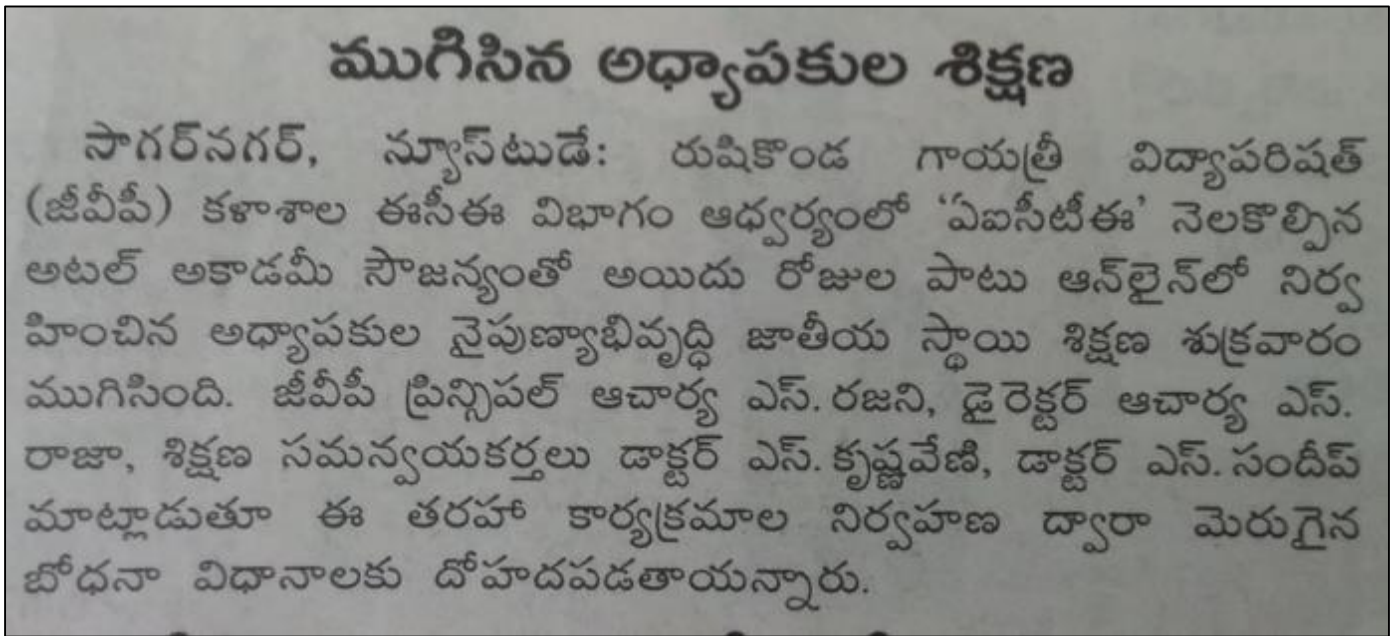
నేటి నుంచి గాయత్రీలో ఫ్యాకల్టీ డెవలప్‌మెంట్ ప్రోగ్రామ్

విశాలాంధ్ర-విశాఖసిటీ: గాయత్రీ విద్యాపరిషత్ డిగ్రీ, పీజీ కళాశాల, ఇంజినీరింగ్ అండ్ టెక్నాలజీ ప్రోగ్రామ్ రుషికొండ ప్రాంగణంలో నవంబరు 2వ తేదీ నుంచి 6వ తేదీ వరకు ఐదు రోజుల ఫ్యాకల్టీ డెవలప్‌మెంట్ ప్రోగ్రామ్ నిర్వహిస్తున్నట్టు నిర్వా హకులు తెలిపారు. ఏఐసీటీఈ అటల్ సహకారంతో కళాశాల ఎలక్ట్రానిక్స్ అండ్ కమ్యూనికేషన్ ఇంజినీరింగ్ విభాగం ఆధ్వర్యంలో నిర్వహిస్తున్న ఈ కార్యక్రమం ఆడ్వాన్సెస్ ఇన్ సెన్సార్ టెక్నాలజీ (ఏఎస్‌టీ 2020) అనే అంశంపై వుంటుందన్నారు. ఈ కార్యక్రమంలో ఆయా రంగాలకు చెందిన పలు పరిశ్రమల, ఇంజినీరింగ్ నిపుణులు, అధ్యాపకులు పాల్గొంటారన్నారు.



నేటి నుంచి జాతీయస్థాయి శిక్షణ

సాగర్‌నగర్: రుషికొండ గాయత్రీ విద్యాపరిషత్ (జీవీపీ) కళాశాల ఈసీఈ విభాగం ఆధ్వర్యంలో సోమవారం నుంచి అయిదు రోజుల పాటు అధ్యాపకుల నైపుణ్యాభివృద్ధి (ఫ్యాకల్టీ డెవలప్‌మెంట్) జాతీయస్థాయి శిక్షణ నిర్వహించనున్నట్లు ప్రిన్సిపల్ ఆచార్య ఎస్.రజని ఆదివారం ఒక ప్రకటనలో తెలిపారు. దేశంలో ఉన్నత ప్రమాణాలతో కూడిన సాంకేతిక విద్యను అందించడానికి 'ఏఐసీటీఈ' నెలకొల్పిన అటల్ అకాడమీ సౌజన్యంతో ఆన్‌లైన్ విధానంలో ఈ శిక్షణ ఉంటుందన్నారు. మరిన్ని వివరాలకు చరవాణి నంబర్లు 7382273337, 9642120033లో సంప్రదించాలని సూచించారు.



ముగిసిన అధ్యాపకుల శిక్షణ

సాగర్‌నగర్, న్యూస్‌టుడే: రుషికొండ గాయత్రీ విద్యాపరిషత్ (జీవీపీ) కళాశాల ఈసీఈ విభాగం ఆధ్వర్యంలో 'ఏఐసీటీఈ' నెలకొల్పిన అటల్ అకాడమీ సౌజన్యంతో అయిదు రోజుల పాటు ఆన్‌లైన్‌లో నిర్వహించిన అధ్యాపకుల నైపుణ్యాభివృద్ధి జాతీయ స్థాయి శిక్షణ శుక్రవారం ముగిసింది. జీవీపీ ప్రిన్సిపల్ ఆచార్య ఎస్.రజని, డైరెక్టర్ ఆచార్య ఎస్.రాజా, శిక్షణ సమన్వయకర్తలు డాక్టర్ ఎస్.కృష్ణవేణి, డాక్టర్ ఎస్.సందీప్ మాట్లాడుతూ ఈ తరహా కార్యక్రమాల నిర్వహణ ద్వారా మెరుగైన బోధనా విధానాలకు దోహదపడతాయన్నారు.

It was a great Initiative by ATAL Academy. I am thankful to AICTE for giving me this opportunity to conduct online FDP for faculty members of technical institute of India free of cost. I got huge response for registration as well as lots of compliment of arranging the online FDP’S, content and hands on.

Three Day Online Faculty Development Program Report on "Antenna Design and Analysis using FEKO" from 22.06.2020 to 24.06.2020

Department of Electronics and Communication Engineering, Gayatri Vidya Parishad College for Degree and PG Courses (A), Rushikonda, Visakhapatnam in association with Altair Fekp Solutions has organized a three day online Faculty Development Program (FDP) on "Antenna Design and Analysis using FEKO" from 22.06.2020 to 34.06.2020.

Principal GVPCDPGC(A) Prof S. Rajani have inaugurated the FDP and has inspired the faculty of various institutions to get the maximum benefit out of the Program in learning and acquiring the inherent knowledge to be delivered by the distinguished speakers from Industry. Prof S. Raja Director Engineering and Technology Program, Gayatri Vidya Parishad College for Degree and PG Courses (A) have addressed the participants about the importance of attending such faculty development programs. Dr. S. Krishna Veni, HOD - ECE have enlightened with the recent and latest developments in the Antenna Design to suite specific applications globally. Coordinators Mr. S. Sandeep, Mr. S. Venkatesh and Mr. M. Sri Suresh have welcomed the participants for the Program and has assured the participants that the resource persons with excellent profile of research would be delivering their best during the sessions of the Program.

An overwhelming response from the faculty of various institutes has marked the significance of the Program. The faculty participants have participated actively and have utilized the opportunity in showing their interest to learn and acquire the latest trends and developments in the field of Antenna Design and their Applications. The participants from various distinguished organizations have attended the Program. A total of 35 participants from various organizations/institutes took part and made the FDP a grand success.

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Mr. S. Venkatesh has conveyed the vote of thanks to the Management of Gayatri Vidya Parishad College for Degree and PG Courses (A), the resource persons from Altair Fekp Solutions and all the participants and the Department of ECE for extending their support to organize the Program.

Gmail fdp

Compose

Inbox 970
Starred
Snoozed
Sent
Drafts 17
More

Meet
Start a meeting
Join a meeting

Chat
Dr. P. A
Sri. P. Padmanabha Reddy

FDP Session 1 Video File

Inbox ×

Mr. Sandeep Sivvam
to ecestaff, pvlnphani, narsi07, balajibalu2511, sarojamandapati, Dr.K.Sum

Dear Participant,

We have uploaded today's FDP session in the google folder, Kindly d folder. The drive link is as given below:

https://drive.google.com/drive/folders/1x8vmNSZj-4_CK-LEMQ-g7

Best Regards,

Mr. S. Sandeep
Assistant Professor,
Department of E.C.E,
Gayatri Vidya Parishad
College for Degree and PG Courses (A),
Ph: +919642120033, +918465925033.

DATE & TIME

22-06-2020 from 9:45 AM to 11:00 AM
23-06-2020 from 10:00 AM to 1:00 PM
24-06-2020 from 10:00 AM to 12:30 PM

Note: Detailed schedule will be mailed to all the participants after successful registration for the FDP.

FDP CONVENER

Dr. S. Krishna Veni, HOD-ECE
Ph: +917382273337
e-mail: drkrishnaveni@gvpcdpgc.edu.in

FDP COORDINATORS

Mr. S. Sandeep, Assistant Professor
Ph: +919642120033
e-mail: sandeep@gvpcdpgc.edu.in

Mr. S. Venkatesh, Assistant Professor
Ph: +919666594294
e-mail: venkateshecep@gvpcdpgc.edu.in

Mr. M. Sri Suresh, Assistant Professor
Ph: +919491358846
e-mail: srisuresh@gvpcdpgc.edu.in

ORGANIZING TEAM

Chief Patrons

Dr. P.S. Rao, President, GVP
Sri. D. Dakshina Murthy, Vice-President, GVP
Secretary & Correspondent, GVP College for Degree & PG Courses (A).
Prof. P.V. Sarma, Vice-President, GVP

Patrons

Prof. S. Rajani, Principal
Prof. D. Saritha, Vice-Principal
Prof. Raja, Director, E & T Program

Executive Committee

Mrs. T.S. Jyothi Lakshmi, Assoc. Professor
Dr. P.A Nageswar Rao, Assoc. Professor
Dr. V. Vijaya Kumar, Sr. Asst. Professor
Mrs. N. Sowmya, Asst. Professor
Mr. Ch. Manohar Kumar, Asst. Professor
Mr. V. Ram Nishanth, Asst. Professor
Mr. A. Mahesh Babu, Asst. Professor

Online Faculty Development Program on

Antenna Design and Analysis using FEKO

22nd June, 2020 to
24th June, 2020

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Program Accredited by NBA)

ENGINEERING & TECHNOLOGY PROGRAM

GAYATRI VIDYA PARISHAD
COLLEGE FOR DEGREE AND P.G. COURSES (A)
(Affiliated to Andhra University & Approved by AICTE)
Accreditted by NAAC | ISO 9001 : 2015
website: www.gvpcdpgc.edu.in

Jointly Organised by the Dept. of ECE and Altair Feko Solutions

Gayatri Vidya Parishad College for Degree and PG Courses was established in 1989 offering B.A., B.Com., B.Sc. and B.B.A. with innovative and restructured combinations including Electronics and Computer Science, in addition to the traditional combinations. Post-Graduate courses were started from 1993-94 in various disciplines. Four programs under Engineering and Technology were added in 2011 with due recognition from AICTE and permanently affiliated to Andhra University. The laboratories are well equipped with up to date equipment and simulation softwares. The students are encouraged to perform experiments by dedicated team of faculty.All the courses are granted autonomy by Andhra University.

VISION OF THE DEPARTMENT

To achieve academic excellence and make significant contribution to the society through quality education and research in the field of Electronics and Communication Engineering.

MISSION OF THE DEPARTMENT

To empower the students with quality education, to achieve excellence in research to develop models that meet the needs of the society and to become team leaders with better communication skills ethics and social responsibility.

FEKO SOFTWARE

FEKO is a comprehensive 3D electromagnetic simulation software suite based on state of the art CEM methods that enable users to solve wide range of EM problems such as antenna design, antenna arrays, antenna placement, RFID, RCS, radomes, pattern synthesis with characteristic mode analysis, EMC / EMI, lightning and cable analysis, Bio - electromagnetics, etc.,

SESSION AGENDA

All the sessions are hands-on and the follwoing topics will be covered in the FDP.

- Simulation Driven Innovation by Altair.
- Computational Electromagnetics for Smart Wireless Devices.
- Introduction To Computational Electromagentics And Solver Selection For Different Applications.
- Microstrip Patch Antenna Design and Optimization.
- Introduction to Characteristic Mode Analysis for Antenna Designs.
- Different Techniques For The Efficient Analysis Of Antenna Arrays
- Antenna Placement Analysis

RESOURCE PERSON

Resources persons from Industry.

WHO CAN PARTICIPATE

Faculty members working in any AICTE approved colleges, Research Scholars, M.Tech students and Employees in Industry by paying the Registration fee of Rs. 150/-.

REGISTRATION PROCESS

Participants should pay the registration fee of Rs.150/- (Rupees One hundred and fifty only) by Account transfer and attach the fee receipt in the google form. The bank details are as follows:

Name of the Account: GVPT IETE STUDENT FORUM

Account Number: 64190618759

IFSC Code : SBIN0040546

Name of the Bank : State Bank of India,
MVP Colony Double Road
Branch, Visakhapatnam

Google form link:
https://forms.gle/H8XXpMDPHcDgPKYW6

INSTRUCTIONS TO PARTICIPANTS

- The participants should fill in the registration form with proper mail ID and are requested to join into the whats app group which will be displayed after the submission of the form to get timely updates.
- The FDP will be held in online mode using Microsoft Teams so we request the participants to download this application in the device from which you wish to join before the start of FDP.
- **Every participant will be given one week free license of FEKO software, so that the participants can practice simultaneously during the FDP session.**
- Meeting links for all the sessions will be shared to all the registered participants on 21th June, 2020 @ 7:00 PM to their registered e-mail id.
- E - certificate will be given only if the participant is present for all the sessions and due submission of feedback form at the end of the FDP.

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GAYATRI VIDYA PARISHAD COLLEGE FOR DEGREE AND PG COURSES (A)
RUSHIKONDA, VISAKHAPATANAM 530045 | website: www.gvpcdpgc.edu.in
(Approved by A.I.C.T.E | Affiliated to Andhra University | Accredited by NAAC | ISO 9001:2015)
ENGINEERING & TECHNOLOGY PROGRAM
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(Program accredited by NBA)

Schedule for Faculty Development Programme on "Antenna Design and Analysis using FEKO" from 22-06-2020 to 24-06-2020

Date	Time	Topic	Meeting Link
22-06-2020 Monday	9:45 AM to 10:00 PM	Inaugural Session	https://teams.microsoft.com/l/meetup-join/19%3ameeting_YzEzNTM4YzYtYzgwOC00ZjkxLThhOWQtMjQ4MWZjZTI5ZjJl%40thread.v2/0?context=%7b%22Tid%22%3a%2296b5396f-cfab-4b10-9fc5-64b20af89867%22%2c%22Oid%22%3a%22b24623e4-60fc-41f6-aa9a-ce87969c7092%22%2c%22IsBroadcastMeeting%22%3atrue%7d
	10:00 AM to 10:20 AM	Simulation driven innovation by Altair	
	10:20 AM to 11:00 AM	Computational Electromagnetics for Smart Wireless Devices	
23-06-2020 Tuesday	10:00 AM to 11:00 AM	Introduction to Computational Electromagnetics and solver selection for different applications	https://teams.microsoft.com/l/meetup-join/19%3ameeting_ZTkyNTA0MGMtODIxNy00ZWMzLTkzMTEtZTBlMDE5NjE3MzMz%40thread.v2/0?context=%7b%22Tid%22%3a%2296b5396f-cfab-4b10-9fc5-64b20af89867%22%2c%22Oid%22%3a%22b24623e4-60fc-41f6-aa9a-ce87969c7092%22%2c%22IsBroadcastMeeting%22%3atrue%7d
	11:00 AM 12:00 Noon	Microstrip Patch Antenna Design and Optimization	
	12:00 Noon to 1:00 PM	Introduction to characteristic mode analysis for antenna designs	
24-06-2020 Wednesday	10:00 AM to 11:00 AM	Different techniques for the efficient analysis of antenna arrays	https://teams.microsoft.com/l/meetup-join/19%3ameeting_YWU5YWE4MDctZmU2ZS00ZjJmLWEzNTktMGVhYWI3NmQ2NWI5%40thread.v2/0?context=%7b%22Tid%22%3a%2296b5396f-cfab-4b10-9fc5-64b20af89867%22%2c%22Oid%22%3a%22b24623e4-60fc-41f6-aa9a-ce87969c7092%22%2c%22IsBroadcastMeeting%22%3atrue%7d
	11:00 AM to 12:00 Noon	Antenna placement analysis	
	12:00 Noon to 12:15 PM	Participant feedback followed by Valedictory.	

Instruction to all the participants:

1. The FDP will be held in online mode using Microsoft teams, so we request the participants to download this application in the device from which you wish to join before the start of FDP.

2. All the participants are requested to join for all the sessions as per the schedule.

3. Participants are requested to login to the Microsoft teams window by entering their name as given in the registration so that it will help us to verify your attendance which is filed in the google sheet. Session wise attendance link will be posted in the chat window during the middle of the session.

4. Participants who wish to ask any queries should post only in the chat window specifying your full name in the relevant field.

For technical support please call:

1. **S. Sandeep,**
   Assistant Professor,
   Ph: +919642120033.

2. **S. Venkatesh,**
   Assistant Professor,
   Ph: +919666594294.

Report on "Innovation to Entrepreneurship ... A journey of excitement" an Impact Lecture Session funded by IIC MHRD on 04.07.2020

An Impact Lecture session on "Innovation to Entrepreneurship ... A journey of excitement" is organized by Department of Electronics and Communication Engineering funded by IIC MHRD to the students of Gayatri Vidya Parishad College for Degree and PG Courses (A) on 4th July, 2020 from 10.30 AM to 2.00 PM. Sri. G. Anantram, Consultant and Content, Developer / Editor for Start-Ups has delivered the lecture as the resource person for the session. The lecture session has been delivered online (as directed to organize by IIC MHRD due to COVID-19) through Teams Microsoft app.

The session has began with an inaugural addressed by Dr S. Krishna Veni; Head, Department of Electronics and Communication Engineering; Prof D. Saritha, Vice Principal, Gayatri Vidya Parishad College for Degree and PG Courses (A) and Prof. S. Rajani, Principal, Gayatri Vidya Parishad College for Degree and PG Courses (A). Mr.V. Ram Nishanth, Assistant Professor has anchored the session introducing the resource person to the students.

The resource person have inspired a brain storming session highlighting about entrepreneurs, startups, patents and finally leading them towards Make in India concept. The speaker narrated the student participants about the various challenges they would be facing ahead and how to resolve them. He added in the present scenario of COVID-19 and its post affects; that all of them have to inculcate innovative ideas that would lead them to become entrepreneurs. The resource person has triggered some of the student participants who are having some ideas of startups. The session went on not only lecturing but also it was an excellent exhibition of an interactive session and solving puzzles. About 257 students from the institution have registered for the impact lecture session.

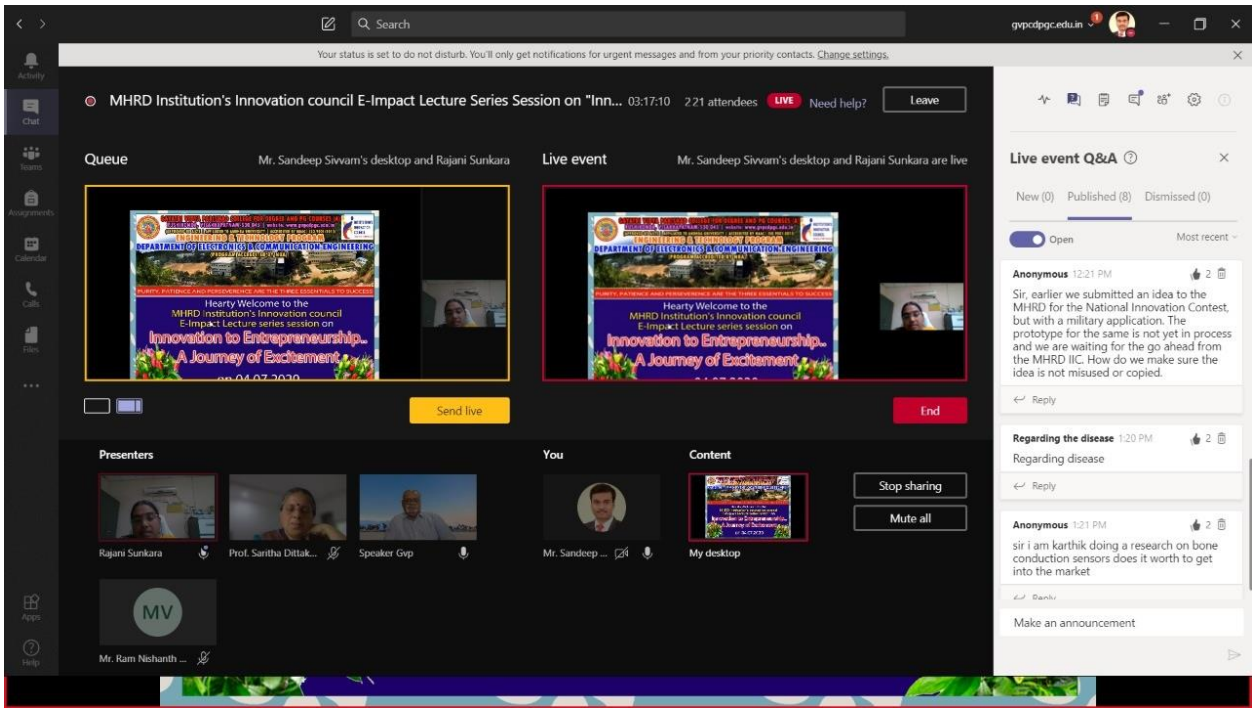
All the students attended the session are highly motivated and had an excellent exposure marching towards the startups. The students clarified many of their doubts by their queuing queries; which all of them were answered by the resource person patiently.

All the students have thanked the department and IIC MHRD for organizing such an excellent impact lecture session which provided them a learning step to march towards Make in India domain of our country. Prof D. Saritha, Vice Principal and President, MHRD IIC, Gayatri Vidya Parishad College for Degree and PG Courses (A) have conveyed that some of the students are approaching IIC MHRD of the institute with new ideas for patents and startups; however they need right guidance and direction to get materialized for the cause and requested the speaker

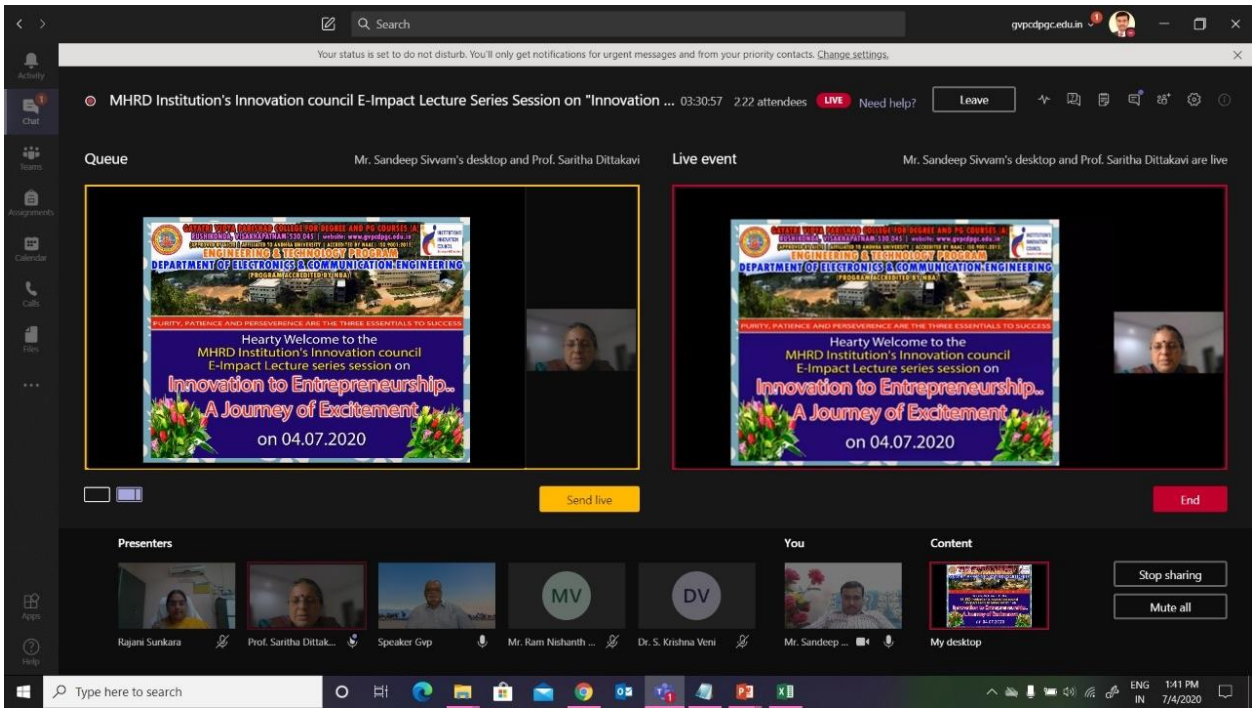
to extend his support in future in filing patents and develop startups. Prof. S. Rajani, Principal, Gayatri Vidya Parishad College for Degree and PG Courses (A) has congratulated the department in organizing the IIC MHRD impact lecture session with a prominent resource speaker Sri. G. Anantram who had made the session interesting to the participants.

Finally vote of thanks by Mr. V. Ram Nishanth expressing a deep sense of gratitude to Sri. G. Anantram; the resource person who have enlightened the participants with his motivating and thought provoking lecture.

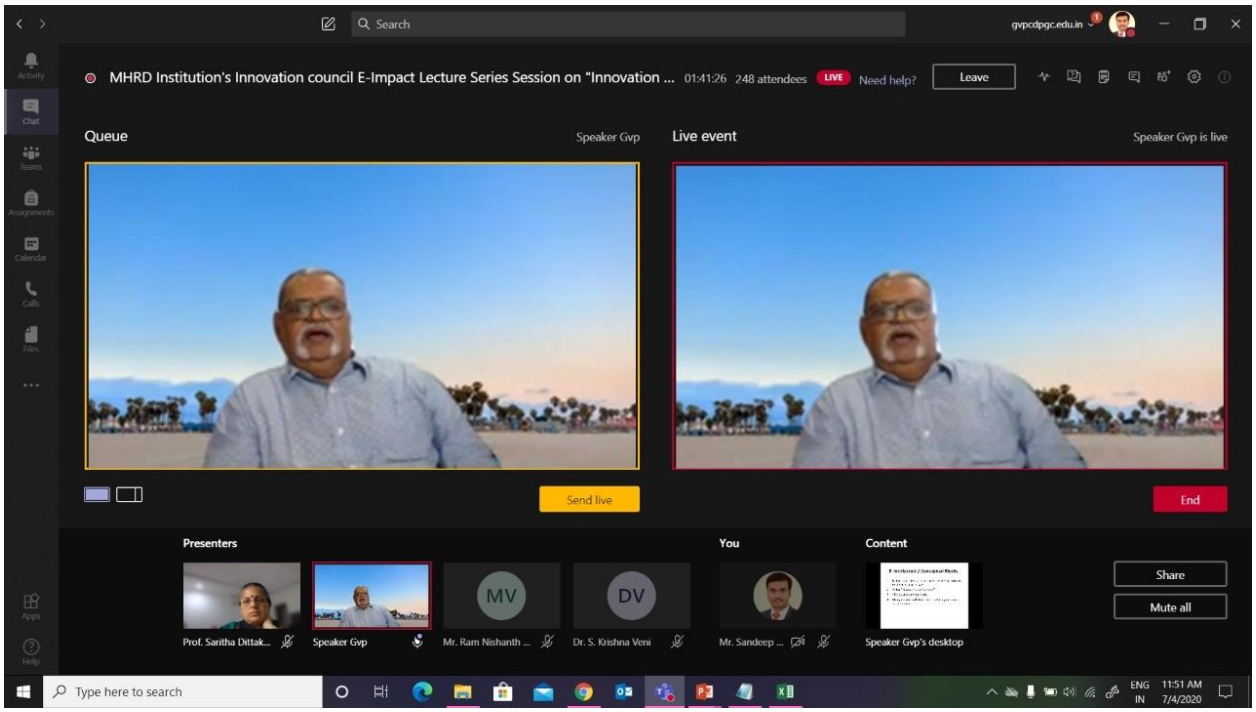
Dr. S. Krishna Veni, HOD-ECE, welcoming the Participants



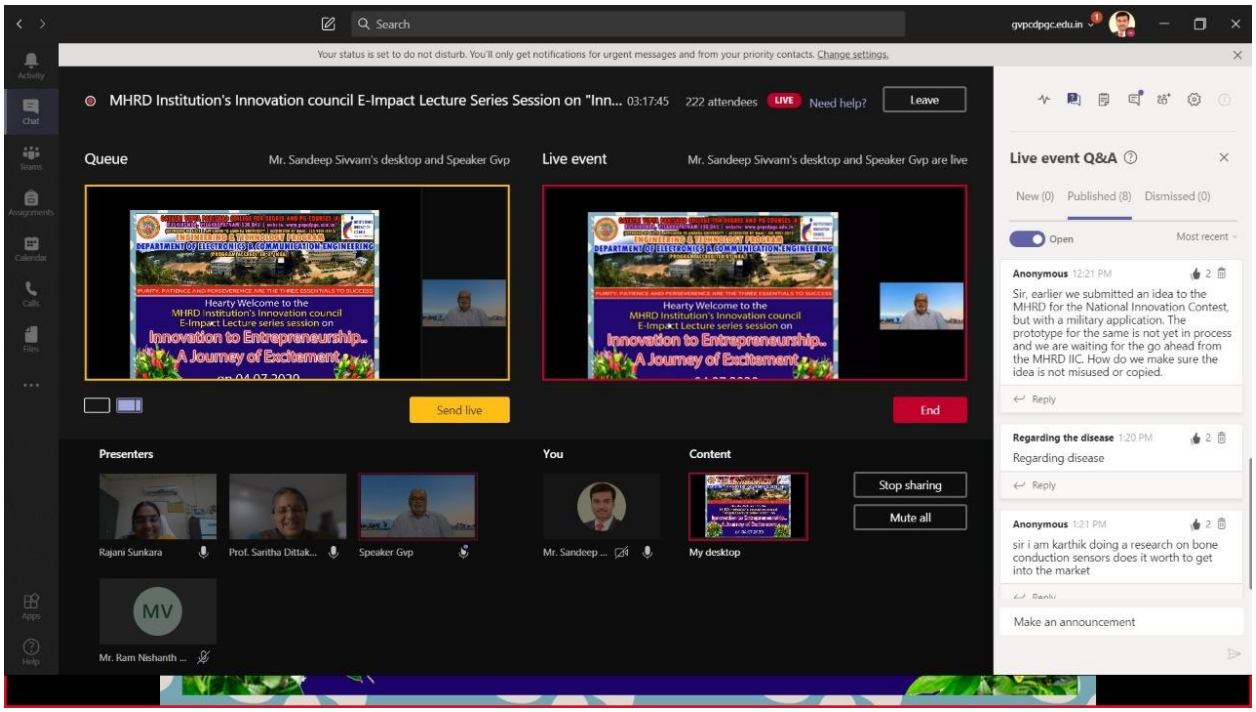
Prof S. Rajani, Principal, GVPCDPGC addressing the session



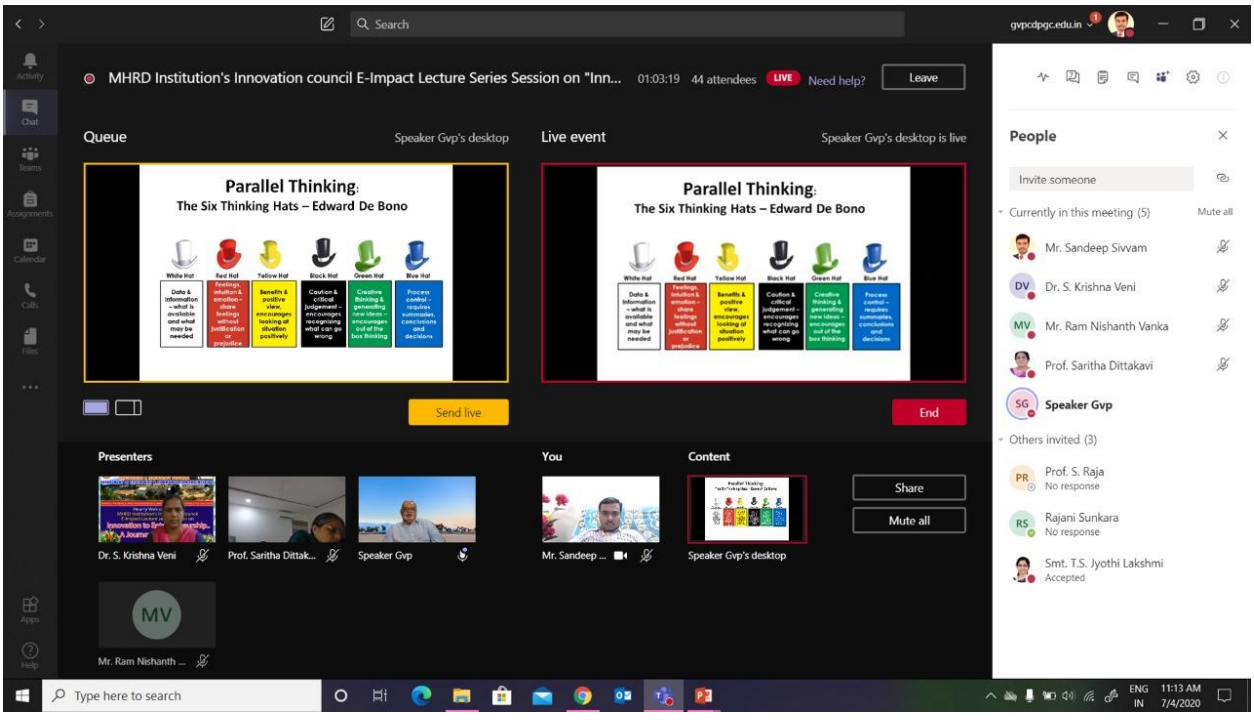
Prof D. Saritha, Vice Principal, GVPCDPGC addressing the session



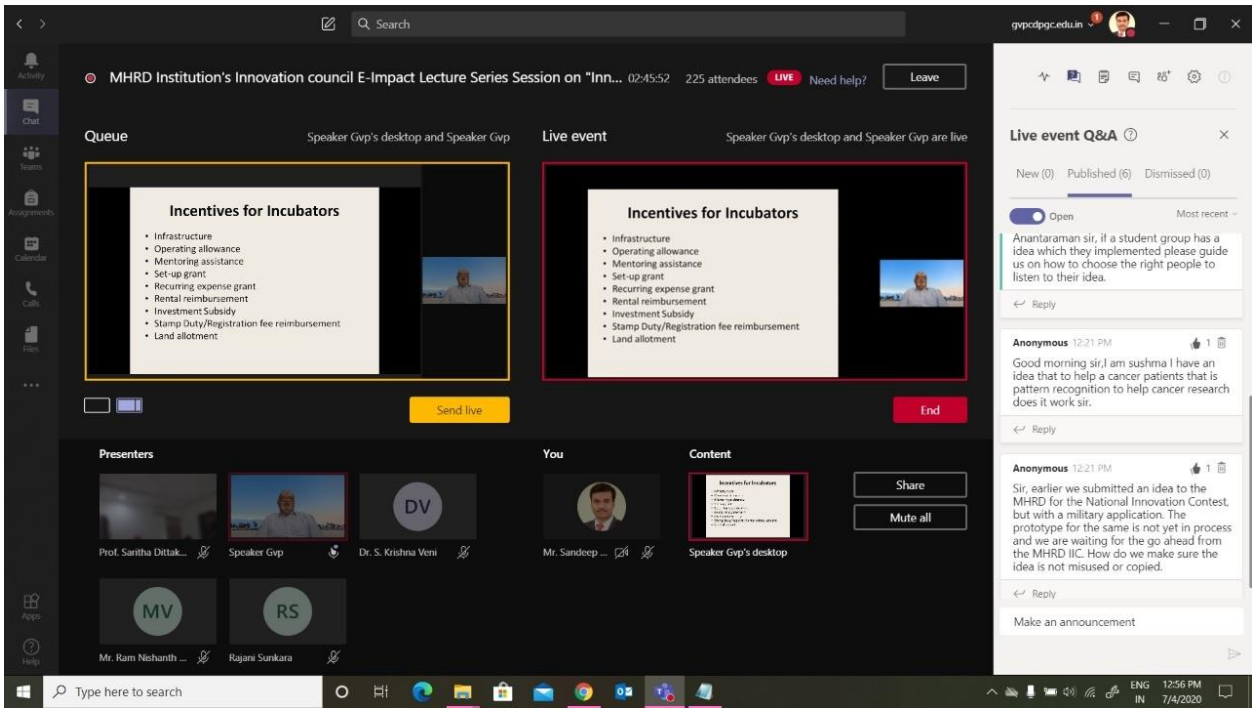
Sri G. Anantram, Resource Person addressing the students



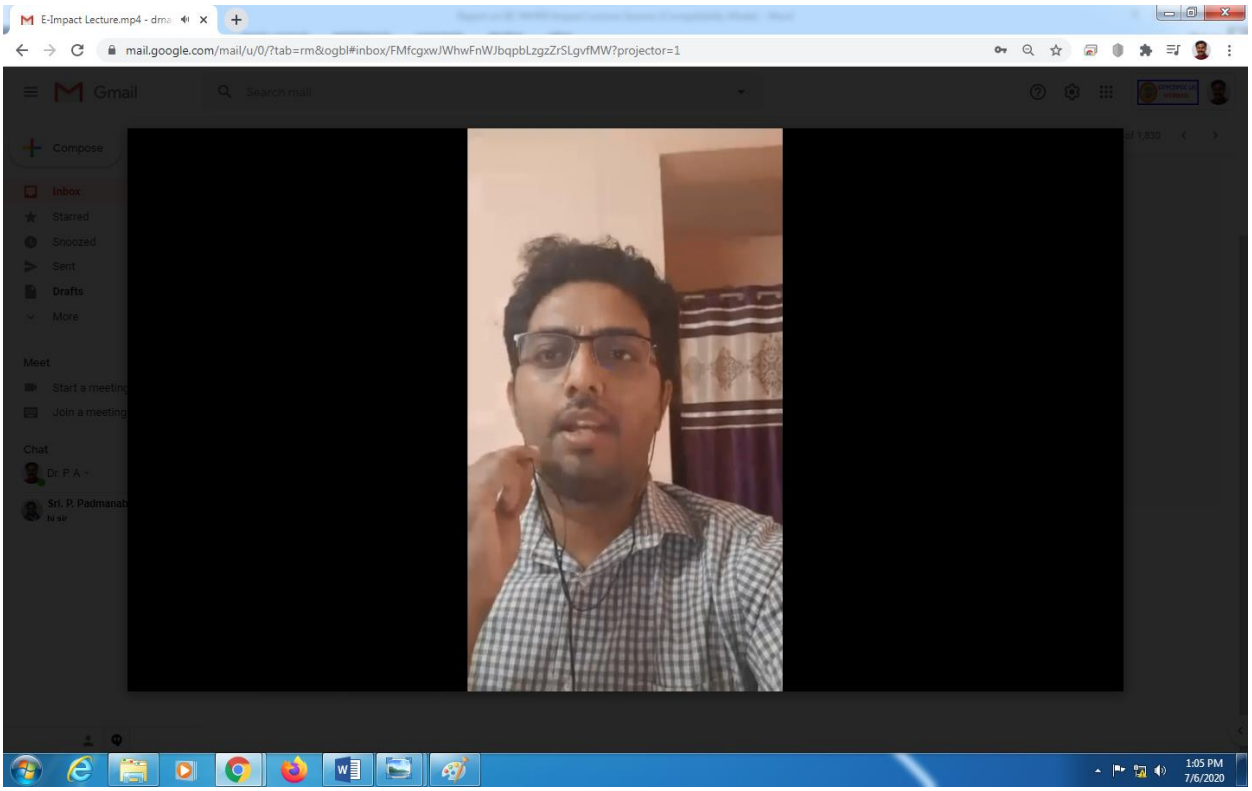
Sri G. Anantram, Resource Person delivering the lecture



Sri G. Anantram, Resource Person delivering the lecture



Sri G. Anantram, Resource Person delivering the students



Mr. V. Ram Nishanth proposing vote of thanks

GVP College for Degree and PG Courses
RUSHIKONDA, VISAKHAPATNAM – 530 045.

Engineering and Technology Program
Department of Electronics and Communication Engineering

Date: 25.01.2021

REPORT ON ONLINE GUEST LECTURE

An ONLINE guest lecture is delivered on "**An Overview of VLSI Design and Opportunities**," by **Avinash Yadlapati**, Senior Director –Engineering, Mirafra Technologies on 25.01.2021. All the students of II and III ECE and faculty of ECE Department have attended the lecture.

The session was an interactive exploring the opportunities in VLSI domain. The resource person presented an excellent vision from the basics and fundamentals of VLSI converging details from the need of VLSI to students towards scope of achieving a career in the VLSI domain.

The resource person had attracted each of the students by his innovative presentation covering the topics Current Trends in VLSI, VLSI Design –Technical Standpoint, Process of VLSI Design, Top-Down Approach, Front-End Design Flow, Design Specification, etc.,

As per the feedback from the students the lecture is very good and informative. They gained lot of information beyond the extent of the bookish knowledge from the resource person.The students have expressed that such lectures from industrial persons are very useful to them. Further they requested the HOD and management to arrange such useful seminars, as many as possible to facilitate them to interact with great professionals and personalities. The students and Faculty of the department have expressed their deep sense of gratitude to **Mr. Avinash Yadlapati** for having accepted our invitation to deliver the lecture.

An Overview of VLSI Design and Opportunities

Avinash Yadlapati

Senior Director – Engineering

Mirafra Technologies

(www.mirafra.com)

Introduction

- VLSI stands for Very Large Scale Integration
- It is primarily related to Electronics field.
- It is also known as Chip Design which has primarily two parts, one is Analog Design and the other is Digital Design.
- Its application is very vast and in other words, every application that is intelligent needs VLSI technology inside it.
- Some examples of VLSI Design applications are Mobiles, Smart watches, Bluetooth, Automobiles etc.

Current Trends in VLSI

- CMOS technology is the current prevailing technology in VLSI due to its high speed and packing density coupled with low power consumption
- The new emerging technologies in VLSI are Bipolar-CMOS and CMOS in silicon on insulator (SOI).
- The latest technology where the Industry is heading to is known as the FINFET technology (Finfet stands for fin field-effect transistor).

VLSI Technology

- VLSI technology is considered to be one of the most core technologies any ECE/EEE engineer would like to work upon.
- Any Electronics engineer's dream job would be a career in VLSI due to the involvement of core electronics subjects like EDC (Electronics Devices and Circuits, CMOS VLSI, Digital Electronics etc.).
- It is called as one of the state of the art technology where very few engineers can get a chance to work in this domain and there are very few engineers who are aware of this field.
- The number of companies in the field of VLSI are very less compared to Software companies due to the requirements of high technology tools and labs required to execute the projects.

VLSI Design – Technical Standpoint

- Integration: Integrated Circuits
  - multiple devices on one substrate
- How large is Very Large?
  - SSI (small scale integration)
    - 7400 series, 10-100 transistors
  - MSI (medium scale)
    - 74000 series 100-1000
  - LSI 1,000-10,000 transistors
  - VLSI > 10,000 transistors
  - ULSI/SLSI (some disagreement)

VLSI Design – Technical Standpoint(Cont)

- But the real issue is that VLSI is about designing systems on chips.
- The designs are complex, and we need to use structured design techniques and sophisticated design tools to manage the complexity of the design.
- We also accept the fact that any technology we learn the details of will be out of date soon.
- We are trying to develop and use techniques that will transcend the technology, but still respect it.

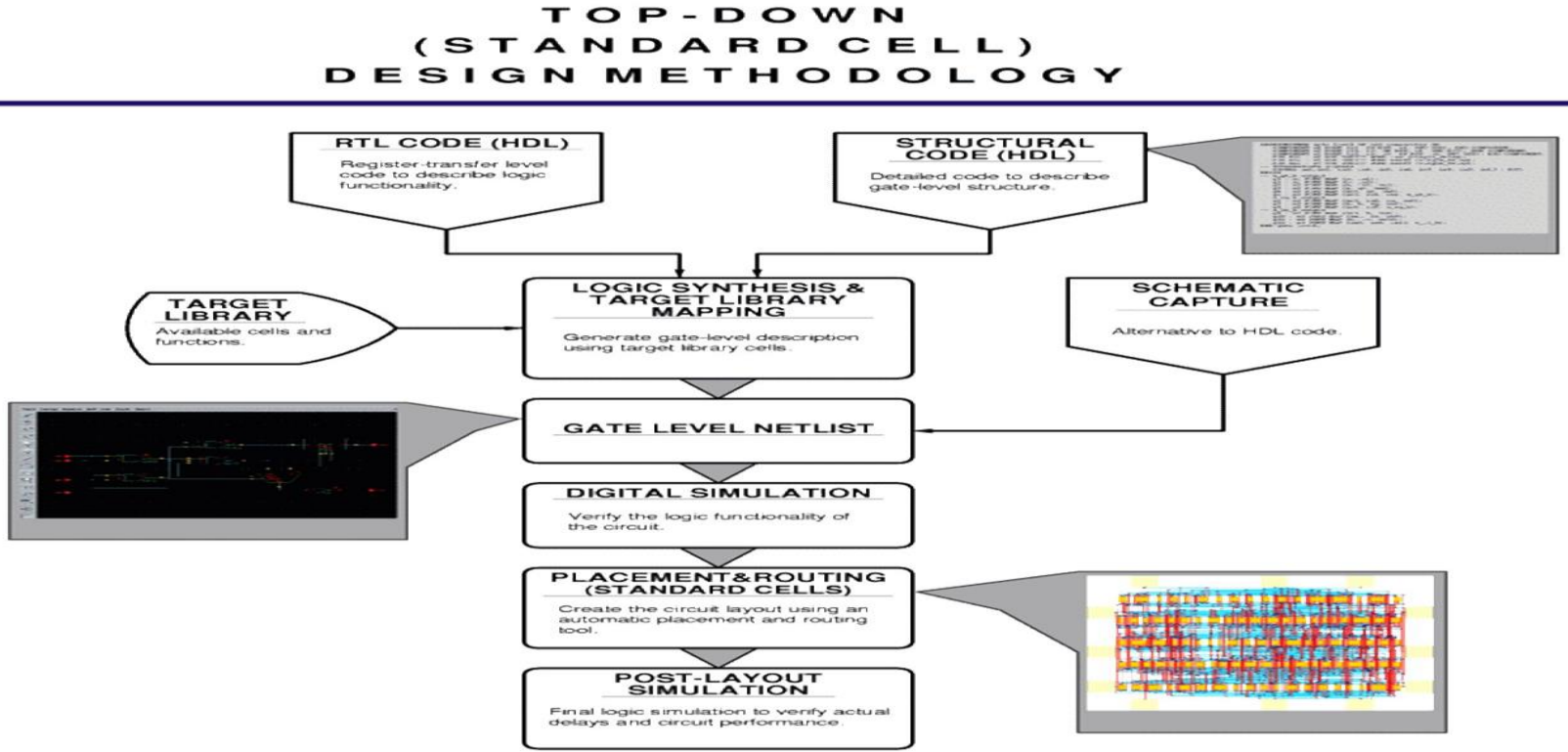
Process of VLSI Design

Consists of many different representations/Abstractions of the system (chip) that is being designed.

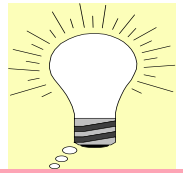
- System Level Design
- Architecture / Algorithm Level Design
- Digital System Level Design
- Logical Level Design
- Electrical Level Design
- Layout Level Design
- Semiconductor Level Design (possibly more)

Each abstraction/view is itself a Design Hierarchy of refinements which decompose the design.

Top-Down Approach

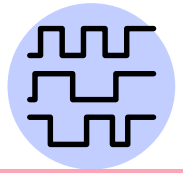


Front-End Design Flow



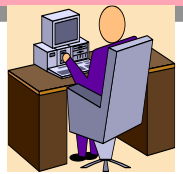
Design Ideas (Specifications)

Detailed (RTL) Design



Functional Simulation

Synthesis & Implementation



Timing Simulation

Device Programming

Design Specification

- What are the main design considerations?
  - Design feasibility?
    - Performance
    - power consumption
    - cost
  - Design spec?
    - Written (Document)
      - Good starting point, but can be misinterpreted by design team
    - Executable (UML, C/C++, Behavioral VHDL, SystemVerilog)
      - Harder to understand, less room for misinterpretation
  - Implementation platform
    - FPGA/CPLD?
    - ASIC?
    - Which FPGA/CPLD vendor?
    - Which device family?
  - Development time?

RTL Specification

- Determine I/O signals
  - Standard interface, protocol, custom interface
- Partition design into functional blocks
  - Datapath, Control logic, Memory, etc.
- Determine block interfaces
- Specify each block separately at RTL
  - MUXs, counters, adders, flip-flops etc.

Detailed Design

- Choose the design entry method
  - Schematic
    - Intuitive & easy to debug
    - Not portable
    - Poor designer productivity (gates/time)
  - HDL (Hardware Description Language), e.g. Verilog, VHDL, SystemC
    - Requires some experience, harder to debug
    - Descriptive & portable
    - Easy to modify
    - Greater productivity
  - Mixed HDL & schematic
- Interpret the specifications
- Manage the design hierarchy
  - Design partitioning
    - Chip partitioning
    - Logic partitioning
  - Use vendor-supplied IP libraries to reduce design time
  - Create & manage user-created libraries (circuits)

Functional Simulation

- Preparation for simulation
  - Generate simulation patterns
    - Waveform entry
    - HDL testbench
  - Generate simulation netlist
- Functional simulation
  - To verify the functionality of your design only
- Simulation results
  - Waveform display
  - Text output
  - Self-checking testbench
- Challenge
  - Sufficient & efficient test patterns

HDL Synthesis

- Synthesis = Translation + Optimization
  - Translate HDL design files into gate-level netlist
  - Optimize according to your design constraints
    - Area constraints
    - Timing constraints
    - Power constraints
- Main challenges
  - Learn synthesizable coding style
  - Use proper design partitioning for synthesis
  - Specify reasonable design constraints
  - Use HDL synthesis tools efficiently

Design Implementation

- Implementation flow
  - Netlist merging, flattening, data base building
  - Design rule checking
  - Logic optimization
  - Block mapping & placement
  - Net routing
  - Configuration bitstream generation (FPGA only)
  - Scan flip-flop insertion (ASIC only)
- Implementation results
  - Design error or warnings
  - Device utilization (FPGA)
  - Die size (ASIC)
  - Timing reports
- Challenge
  - How to reach high performance & high utilization implementation?

Common Pitfalls

- Not detailed enough specifications
  - **Do not start** design entry until all details are clear
  - A poor design cannot be saved by good code and synthesis/implementation constraints
  - Sometimes though, it **is better** to let the tool do the optimization (for example state machines)
- Always remember that you cannot **prove** a complex design has no bugs
- For complex designs, verification (simulation) and redesign is 80% of total design time!

Gate-Level Simulation

- Post-layout simulation
- Includes component and wire delays, clock skew, setup and hold times
- Same input vectors with functional simulation
- It is necessary even if Static Timing Analysis shows no problems

Opportunities in VLSI

1. There are multiple opportunities in VLSI for freshers.
2. They can either go in Front-end VLSI design or Back-End Design.
3. They can also go into other domains like Analog Layout, Design, PCB Design etc.
4. They need to take training in the respective area of their interest before they start looking for opportunities.
5. They need to be technically strong in Digital Design, EDC, CMOS VLSI, Microprocessor and Analog Design.

Entry Level Position

1. Any fresh graduate from ECE or EEE will enter as VLSI Trainee Engineer or Design Engineer – I
2. A fresh post graduate with M.Tech may enter as direct engineer with grade Design Engineer.

Senior Engineers Role

1. A Senior engineer is responsible to execute multiple tasks or even projects.
2. He is also responsible to train the junior engineers who come from colleges.
3. More senior roles will demand leadership skills like technically leading a team, mentoring the juniors, communicating with the senior management etc.

Manager Role

1. There are multiple roles at managers or Senior Management functions.
2. They are responsible for the overall functioning of the company including the revenues and profits.
3. They are responsible to recruit good and quality engineers who can learn quickly and adapt themselves to the company environment.
4. They are responsible for overall quality assurance for all the projects that are executed.

Detailed Opportunities

- Opportunities are present in VLSI Front-End
- Opportunities are present in VLSI Back-End
- Opportunities are present in Analog Layout
- Opportunities are present in Analog Design
- Opportunities are present in FPGA
- Opportunities are present in Board Design
- Opportunities are present in Post Silicon Validation
- Opportunities are present in Testing of VLSI Circuits

VLSI Front End Opportunities

- RTL Design (Verilog/VHDL/System Verilog)
- Verification

-> RTL Verification

-> Gate Level Verification

-> Verification with SDF (Back Annotated Netlist)

- Synthesis and STA (Static Timing Analysis)
- Formal Verification (LEC and Assertions)
- Lint and Clock Domain Crossing Verification
- Low Power Verification (UPF and CPF)

VLSI Back-End Opportunities

- Place and Route (P&R) Engineers
- Physical Design CAD Engineers (Tool flow)
- Physical Design Application Engineers for EDA companies like Synopsys, Cadence and Mentor Graphics
- Timing Engineers (STA- Post Layout) with SI checks (Signal Integrity)
- Low Power PD
- IR Drop Specialists
- Full Chip PD and STA engineers

VLSI Analog Layout Engineers

- Layout Engineers who have good understanding of layout concepts like stick diagrams.
- They need to be good at CMOS VLSI.

VLSI Analog Design Engineers

- Layout Engineers who have good understanding of Analog Design concepts like PLL, OpAmp's concepts.
- They need to be good at CMOS VLSI Design.
- Some examples of Analog Design are:

-> Resistors

-> Capacitors

-> Diodes

-> Transistors

-> Operational Amplifiers

VLSI FPGA Engineers

- FPGA Engineers should have good understanding of concepts like different FPGA architectures (Xilinx, Altera etc), RTL Coding, Synthesis and Implementation.
- They need to be good at verification and validation.
- Some common types of FPGA's used in the Industry are:

-> Xilinx

-> Altera

VLSI Board DesignEngineers

- Board Design engineers should be typically good at PCB.
- They should be aware of different architectures and applications.

VLSI PSV Engineers

- Post Silicon Validation Engineers are heavily in demand now in the Industry.
- They should be good at Validation (Using Testers).
- They should be good at Emulation.
- They should be good at C.
- They should have worked in product companies and used validation tools like Palladium.

VLSI Companies

- Semiconductor companies

2001 Rank	Company	2001 Sales
1	Intel	23.5
2	ST Micro	6.4
3	Toshiba	6.1
4	TI	6.0
5	Samsung	5.2
6	Motorola	4.8
7	NEC	4.8
8	Infineon	4.6
9	Philips	4.4
10	AMD	3.9

- Fab-less “Design Houses”

2001 Rank	Company	2001 Sales
1	Qualcomm	1.24
2	Nvidia	1.21
3	Xilinx	1.15
4	Via	1.01
5	Broadcom	0.96
6	Altera	0.84
7	Cirrus Logic	0.53
8	ATI Techn	0.52
9	Media Tek	0.45
10	QLogic	0.36

Thank You

Dr. Avinash Yadlapati

M.Tech, Ph.D

SENIOR DIRECTOR - ENGINEERING
Mirafra Technologies
Hardware Engineering Division
Hyderabad
Telangana, India
avinashy@mirafra.com
Mobile No: +91-9989835092

EXPERIENCE SUMMARY:

- Having close to 20 years of Industry experience in VLSI Design experience from RTL to GDSII in lower nodes like 10nm and 7nm technologies.
- **Currently working as Senior Director-Engineering, Mirafra Technologies** (www.mirafra.com) since February 2018, Hyderabad.
- Past experience in companies like Infosys, Cyient, AMD, Qualcomm and HCL Technologies.
- Working as "Visiting Faculty" at BVRIT-Narsapur since June-2015.
- Working as "Visiting Faculty" at BITS Pilani Hyderabad.
- Board of Studies member at BV Raju Institute of Technology, Narsapur and Annamacharya Institute of Technology and Sciences, Rajampet.

ACADEMIC PROFILE:

Degree Awarded	Institution	University	Year of Completition
Ph.D (ECE)	K L University	K L Deemed to be University	2020
M.Tech (VLSI)	K L University	K L Deemed to be University	2015
M.Sc (Electronics)	Andhra University	Andhra University	1999

TECHNICAL SKILLS:

- Verification Tools : Cadence NCSim, Synopsys VCS/VCSMX
- Synthesis Tools : Synopsys Design Compiler, Cadence RC
- Linting Tools : LEDA, Spyglass
- Timing Tools : Einstimer, PrimeTime
- Logic Equivalence : Cadence LEC
- Scripting : Shell, Perl
- Protocols : AMBA AHB, OCP, AXI, USB 2.0, CAN, PCI

FIELDS OF INTEREST:

- RTL Design using Verilog/VHDL
- Logic Synthesis of Digital Circuits using Synopsys DC.
- Design for Testability
- CMOS VLSI Design
- Advanced Digital Logic Design
- Design with PLDs and FPGAs
- VLSI Testing Circuits
- Microprocessors and Microcontrollers

MEMBERSHIPS IN PROFESSIONAL BODIES/SOCIETIES/ORGANISATIONS

- Senior Member, IEEE

ACHIEVEMENTS & AWARDS:

- Instrumental in setting up "Cyient Incubation Center" at BV Raju Institute of Technology, Narsapur
- Got an Award from BVRIT Chairman for valuable contributions at BVRIT
- Placed more than 100 BVRIT students in core jobs like VLSI

TEACHING –MAJOR SUBJECTS HANDLED

- Advanced Digital Logic Design, Verilog, Synthesis and STA, Digital Integrated Circuit Design with PLDs and FPGAs, MOS Circuit Design, CMOS VLSI Design, Design for Testability

Books Published

- Book Name "**AN EXPERIMENTAL APPROACH TO VLSI SYSTEM DESIGN**", ISBN-13: 978-9386258-85-4, VSRD Academic Publishing-December 2017.

International Journal Papers PUBLISHED

2019

1. Avinash Yadlapati, **Hari Kishore Kakarla "Design and Verification of Asynchronous FIFO with Novel Architecture Using Verilog HDL"** Journal of Engineering and Applied Sciences **(Scopus)**, ISSN No: 1816-949X, Vol No: 14, Issue No: 1, Page No: 159-163, January 2019.
2. Avinash Yadlapati, **K Hari Kishore "Implementation of Asynchronous FIFO using Low Power DFT"** International Journal of Innovative Technology and Exploring Engineering (IJITEE)**(Scopus)**, ISSN: 2278-3075, Volume-8, Issue No: 6S, Page No: 152-156, April 2019.
3. Avinash Yadlapati, **Hari Kishore Kakarla "Low-power design-for-test implementation on phase-locked loop design"** Measurement and Control **(SCIE)**, ISSN: 0020-2940, Volume-52, Issue No: (5-6), Page No: 106-109, June 2019.

2018

4. Avinash Yadlapati**, K Hari Kishore** "**Low Power Synthesis for Asynchronous FIFO using Unified Power Format (UPF)**" International Journal of Engineering and Technology(UAE) **(Scopus)**, ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 7-9, March 2018
5. Avinash Yadlapati, **K Hari Kishore "System Level Verification of Advanced Extensible Interface Protocol Using Verilog HDL"** Journal of Advanced Research in Dynamical and Control Systems **(Scopus)**, ISSN No: 1943-023X, Vol No: 10, Special Issue No: 7, Page No: 1359-1365, June 2018.

2017

6. Y Avinash, **K Hari Kishore** ‘’**Designing Asynchronous FIFO for Low Power DFT Implementation**’’ International Journal of Pure and Applied Mathematics **(Scopus)**, ISSN No: 1314-3395, Vol No: 115, Issue No: 8, Page No: 561-566, September 2017

2016

7. Avinash Yadlapati**, Hari Kishore Kakarla** "**Validating Advanced Extensible Interface Protocol using Randomized Verification Environment**" International Journal of Engineering and Technology **(IJET- *Non Scopus*)**, ISSN No: 2395-1303, Vol No.02, Issue No.03, page: 01-08, May-June 2016

8. Sravya Kante, **Hari Kishore Kakarla**, Avinash Yadlapati,"**Design and Verification of AMBA AHB-Lite protocol using Verilog HDL**" International Journal of Engineering and Technology **(IJET-*Scopus*)**, E-ISSN No: 0975-4024, Vol No.8, Issue No.2, Page:734-741, April-May 2016.

2015

9. Avinash Yadlapati, **Dr. Hari Kishore Kakarla**, “**An Advanced AXI Protocol Verification using Verilog HDL”**, Wulfenia Journal **(SCI-E)**, ISSN: 1561-882X, Volume 22, Number 4, pp. 307-314, April 2015 **(IF-0.649)**

PARTICIPATED IN NATIONAL/INTERNATIONAL CONFERENCES

2017

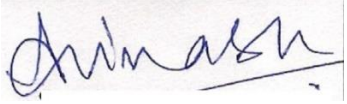
1. Avinash Yadlapati, **Kakarla Hari Kishore**,“**Constrained Level Validation of Serial Peripheral Interface Protocol**”, Proceedings of the First International Conference on SCI 2016, Volume 1, Smart Computing and Informatics, Smart Innovation, Systems and Technologies 77 (Publisher: Springer Nature Singapore Pte Ltd), ISSN No: 2190-3018, ISBN: 978-981-10-5544-7, Chapter No: 77, pp. 743-753, 25th December 2017. **(SCOPUS) (DOI: 10.1007/978-981-10-5544-7_73)**

PARTICIPATED IN WORKSHOPS/SCHOOLS/ACTIVITIES

- Conducted IEEE workshops in various colleges like Osmania University College of Engineering, ECE Department, Gitanjali College of Engineering and Technology, Muffakham Jah College of Engineering and Technology.

REFERENCES:

Dr.Kakarla Harikishore **Professor and Associate Dean (Student Affairs),** **Department of ECE** K L Deemed to be University, Guntur Andhra Pradesh	**Dr. I.A.Pasha** **ECE HOD** BVRIT Narsapur Medak District Telangana



(Dr. Avinash Yadlapati)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
ENGINEERING AND TECHNOLOGY PROGRAM
GAYATRI VIDYA PARISHAD COLLEGE FOR DEGREE & P.G. COURSES (A)
RUSHIKONDA, VISAKHAPATANAM-530045 | WEBSITE: www.gvpcdpgc.edu.in
(Approved by A.I.C.T.E | Affiliated to Andhra University | An ISO 9001:2015 Certified Institute)

Report on Workshop conducted

Title: Three days workshop on Applications of Signal and Image Processing.

Date(s): 28th -30thDecember
Resource Person: J. Prem Kumar,
(Product Manager for Math works Products, Capricot Technologies Pvt.Ltd)

Introduction:

Aiming to provide Practical overview of working on Signal and Image Processing applications through MATLAB 2020 software, a virtual three-day workshop on 'APPLICATIONS OF SIGNAL AND IMAGE PROCESSING' held during 28th to 30 December at 3pm – 5pm conducted by Gayatri Vidya Parishad College For Degree and PG courses, Engineering and Technology program, Department of Electronics and Communication Engineering.The Event is coordinated by Mr.Ram Nishanth V, Asst.Prof. , Department of ECE.

Contents:

- Working of filters
- Simulink tool
- Different Audio and Image Acquisition tool box
- Various Signal processing examples
- Images Processing techniques

Discussion:

On Day-1, the Spokesperson Mr.Prem kumar J, product Manager for Mathworks products, capricot technologies pvt.ltd gave the insights of MATLAB software applications and the add-on tools required for the processing applications and how write the codes in the matlab IDE. Then it is followed by learning the key-points like

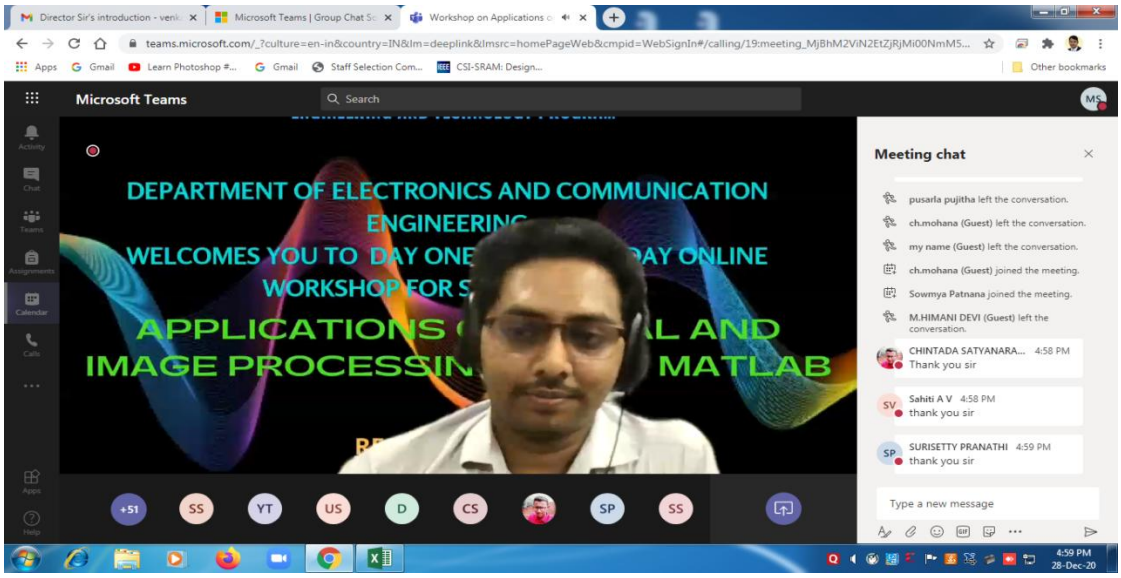
- How to use Simulink tool to perform the signal processing with the example using microphone connected to speaker in a virtual medium through matlab software.
- Observing the process of designing and application of various filters like how the low pass, band-pass filters operating on band limited signals to enhance the signal quality and removing the noise from the filter.
- Brief knowledge on the usage of the Audio System tool box and Digital Signalling system tool box.
- How to access the audio data through the matlab commands that are done by the "Data Acquisition Tool box Support".

On Day-2, the Session was dealt with the different Image processing Application in the matlab like

- How an image can be accessed through same Image acquisition commands and how to process the range intensities and dimensions of the image.
- Method of performing the RGB colour models on images and radiating the certain regions for scanning and analysing the regions for better understanding of the image.
- How to analyse the image through histogram
- The way of performing the sharping of the
- Process of manipulating the images for the further research purpose.
- Hands on Experience of image segmentation and the different methods for segmenting the image.
- Overview of the image tool box implementations of the image processing

Finally the speaker summarized the future applications of the signal and image processing and the fields they are utilized. He also stated how they are helpful in the career point of view.

The following last day where the session is concluded by the assessment on for testing the knowledge throughout the workshop.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DEPARTMENT OF ELECTRONICS AND COMMUNICATION
ENGINEERING
WELCOMES YOU TO DAY ONE
DAY ONLINE
WORKSHOP FOR S
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MATLAB
Meeting chat
pusarla pujitha left the conversation.
ch.mohana (Guest) left the conversation.
my name (Guest) left the conversation.
ch.mohana (Guest) joined the meeting.
Sowmya Patnana joined the meeting.
M.HIMANI DEVI (Guest) left the conversation.
CHINTADA SATYANARA... 4:58 PM
Thank you sir
Sahiti A V 4:58 PM
thank you sir
SURISETTY PRANATHI 4:59 PM
thank you sir
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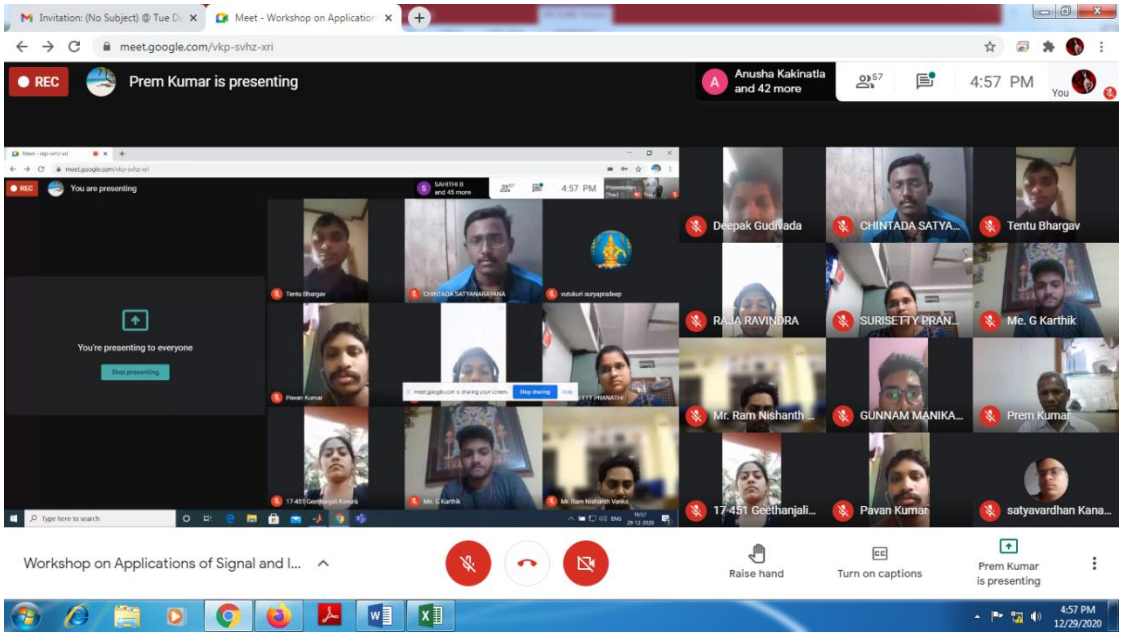
4:59 PM
28-Dec-20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Prem Kumar is presenting
Anusha Kakinatla and 42 more
4:57 PM
You
You're presenting to everyone
Deepak Gudnada
CHINTADA SATYA...
Tentu Bhargav
RAJA RAVINDRA
SURISETTY PRAN...
Me. G Karthik
Mr. Ram Nishanth ...
GUNNAM MANIKA...
Prem Kumar
17-451 Geethanjali...
Pavan Kumar
satyavardhan Kana...
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Prem Kumar is presenting
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12/29/2020